THE CATHOLIC UNIVERSITY OF AMERICA

Architecture and Protocol for Optical Packet Switching

A DISSERTATION

Submitted to the Faculty of the

Department of Electrical Engineering and Computer Science

School of Engineering

Of The Catholic University of America

In Partial Fulfillment of the Requirements

For the Degree

Doctor of Philosophy

By

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Washington, D.C.

2011

Architecture and Protocol for Optical Packet Switching

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This dissertation proposes a number of single and parallel processor architectures and protocols for optical packet switching in all optical networks making use of a number of recent advances in high speed processors and optical buffers and a number of packet contention resolution techniques in wavelength, time, and space, alternative routing and processing speeds. The input and output lines can transmit multiple wavelengths per line (i.e., wavelength division multiplexed lines). In the developed architectures the header of a packet is separated from the body and is processed for determining the route and wavelength to be used to transmit the packet. The body is delayed for as long as is needed for processing the header. Thus only a portion and not the whole packet need to be saved. This reduces buffer size requirement. The optical packet switch also utilizes dynamically updated Link & Channel Availability Tables and dynamically updated hierarchical Routing Tables (OSPF, Next Best Route). Thirteen different Single Input Processor architectures and the Parallel Input Processor architectures are developed and evaluated with and without packet contention resolution techniques. Parallel processors are used at the output in all architectures except one. The various architectures are simulated by using OPNET software simulation package and their performance is evaluated from these simulation results in terms of packet loss rate, average throughput per line and total throughput. Many of the architectures did not provide acceptable performance. The Parallel Input Processor architecture with the number

of wavelength converters equal to the number of input channels and Parallel Input Processor with Next Best Route are shown to provide the best performance (nearly zero packet loss) when using 10 gigabit per second processors for 10 gigabit per second input line rates. Higher rate input lines can be accommodated by down multiplexing the incoming data into 10 gigabit streams and parallel processing these streams. These results are presented on graphical forms. The results of this dissertation will lead to implementation of optical packet switching with its resultant benefits to the all optical networking.

This dissertation by Lesley R.M. Condiff fulfills the dissertation requirement for the doctoral degree in Electrical Engineering approved by Mohammad Arozullah, Ph.D., as Director, and by Sameh Eisharkawy, Ph.D., and Mark Mirotznik, Ph.D. as Readers.

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List of Abbreviations

2X – two times
ASIC – Application-specific Integrated Circuit
BCAM – Binary content addressable memory
BER – Bit Error Rate
CA – Channel Availability
CAM – Content addressable memory
Db - decibels
DWDM – Dense Wavelength Division Mutlitplexing
FIFO – First in, first out
FS – Forwarding Speed
Gbps – Gigabits per second
GHz - Gigahertz
GMPLS – Generalized Multi Protocol Lambda Switching
IP – Internet Protocol
IPv6 – Internet Protocol version 6
ITU – International Telecommunication Union
LUT – Look up table
Mlps – Mega Look-ups per second
mm - millimeters
MPLS – Multi Protocol Lambda Switching
NBR – Next Best Route
Ns – nano seconds
O/E/O – optical-electrical-optical conversion
OL - Output Line Buffer
OSPF – Open Shortest Path First
PBRS – Pseudorandom binary sequence
PPP – Point-to-Point
PS - Picoseconds
RAM – Random access memory
TCAM – Ternary addressable memory
V – Volts
W – watts

Chapter 1 Introduction

This dissertation proposes a number of single and parallel processor architectures and protocols for optical packet switching in all optical networks making use of a number of recent advances in high speed processors and optical buffers and a number of packet contention resolution techniques in wavelength, time, and space, alternative routing and processing speeds.

1.1 All Optical Networks

In all optical networks, electrical information is converted into optical form at the source. The information remains in optical form during its transmission to the destination. There is no optical to electrical to optical (O/E/O) conversion at the intermediate nodes. All switching, amplification and buffering are to be done in the optical domain. There are two ways of information transmission, namely using end to end optical light path establishment and optical packet switching. In the past optical packet switching has been difficult to implement due the lack of availability of optical buffers of required size. Thus emphasis has been given to light path establishment before transmitting information. However, optical packet switching provides a number of advantages over the light path establishment method. Firstly, in a large network a light path may consist of interconnection of a number of optical links. Thus establishment, maintenance and simultaneous obligation of all required resources over long light paths may be problematic. This is not required for packet switching. In packet switching packets are transmitted and switched dynamically at each node using the resources

available at that node. At any time only the resources needed for connecting to the next node are obligated. Secondly, In case of congestion a new light path may be needed to be established. Thus in a heavily loaded network frequent establishment and reestablishment of such light paths are needed. On the other hand in packet switching packets can be dynamically routed around congestion by updating routing tables at the nodes. This may lead to lower delay for packets. Thirdly, packet switching uses fewer resources as at any time only the resources between a transmitting node and the next node are in use, whereas in light path method all the resources between all the nodes in a light path are in use as long as the light path is maintained. Fourthly, in light path establishment method sometimes resources may be not be utilized as the whole path need to be maintained irrespective of whether data is transmitted over it or not, whereas in packet switching resources are obligated only when they are used.

Many current deployed optical networks use wavelength division multiplexing (WDM). WDM is based on frequency division multiplexing. In frequency division multiplexing, the bandwidth of a channel is divided into multiple channels. Each channel occupies part of the larger frequency spectrum. WDM has similar concepts. A channel is called a wavelength. This terminology comes from each channel at a different wavelength. Wavelengths on optical fiber are separated by unused optical spectrum.

Figure 1 illustrates a simple example of a WDM link. Four optical fibers are connected to a WDM multiplexer. The WDM multiplexer combines or multiplexes the four optical fibers into one optical fiber. The inverse operation occurs at the receiving multiplexer. The receiving multiplexer is commonly called a demultiplexer. The demultiplexer separates the wavelengths and sends the wavelengths to an appropriate output port. The output port may be another optical fiber.

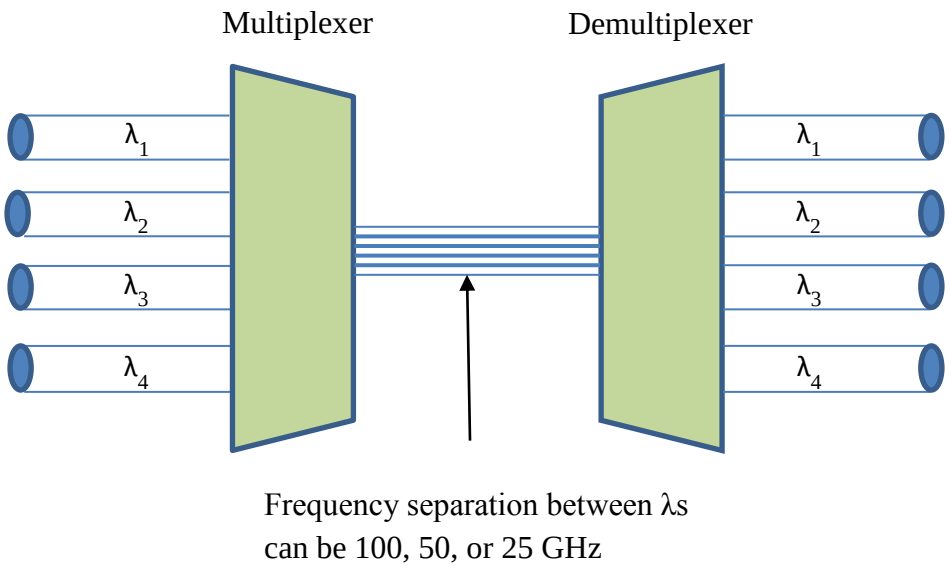

Figure 1 A Wavelength Division Multiplexing Link

As Figure 1 illustrates, each wavelength is separated by unused optical spectrum. This prevents the signals from interfering with each other signal. The International

Telecommunication Union (ITU) has published standards on the spacing. The most common spacing is 100 GHz spacing. This was specified in the first ITU-T specification for WDM in Recommendation G.692, Optical Interfaces for Multichannel Systems with Optical Amplifiers. Recommendation G.692 has alternative spacing of 50 GHz and 200 GHz. Recommendation G.692 applies to 4, 8, and 16 channel WDM systems [1]-[4].

Dense Wave Division Multiplexing (DWDM) has the multiplexing of more than 160 channels with data rates of 10 gigabits per second (Gbps). The channel spacing for DWDM is 25 GHz. The total data rate for 160 channel DWDM system is 1.6 terabits per second (Tbps). DWDM systems with 320 channels and a total data rate of 3.2 terabits have been proposed [1]- [3].

Currently, in order to perform switching in WDM systems, optical packets must be converted to electrical packets. The electrical packet is then forwarded to the appropriate output port. The electrical packet is then converted back to an optical packet. Electrical switches and routers cannot forward packets at the data rates required by DWDM systems. This is commonly known as the optical electrical optical (O/E/O) bottleneck..

In all optical networks, electrical information is converted into optical information at the source. The information remains optical information during the transmission to the

destination. There is no optical to electrical to optical (O/E/O) conversion at the intermediate nodes. All switching, amplification and buffering needs to be done in the optical domain.

An all-optical network will provide fast automatic setup and teardown of paths across the optical network. This requires an implementation of a dynamically reconfigurable optical transport layer based on fast optical cross connects (OXCs) that are coupled with a suitable control and management architecture. The optical transport network (OTN) will be capable of supporting large numbers of high-capacity channels with data rates on the order of 10 – 40 gigabits per second (Gbps) [5].

Additional information on all-optical packet switched networks can be found in [6]-[12].

1.2 Typical Optical Network

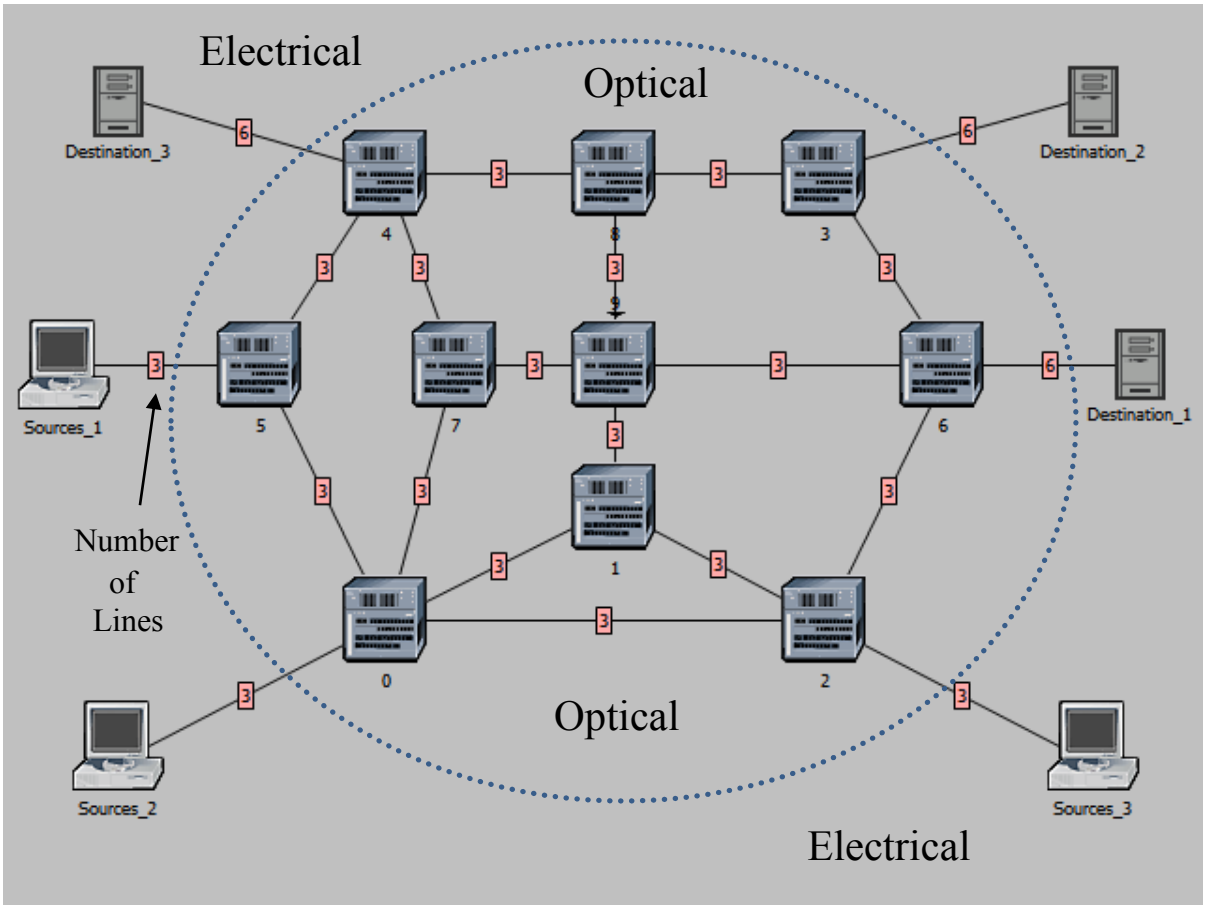

Figure 2 A Typical All Optical Network

The typical optical network is shown above in Figure 2. The typical optical network has a number of sources and destinations that are connected to it. The all optical network contains a number of optical switches, multiplexers, and demultiplexers. Add the functions of the switches. The sources and destinations process packets electrically. Packets are generated electrically at the source. The packets undergo an electrical to optical conversion after packets leave the source. The packets are forwarded and routed optically. The packets are

converted from being an optical packet to an electrical packet at the last hop to the packet's destination.

1.3 Modes of Operation- Advantages of Optical Packet Switching

The modes of operation are light path switching (circuit switching) and packet switching.

Light path switching requires end-to-end light paths to be established, maintained, and terminated. Resources need to be reserved for the entire light path. Light path switching uses Generalized Multiprotocol Label Switching Protocols (GMPLS) and reservation protocols to reserve resources. Difficulties exist in the establishment and maintenance of many required light paths that are simultaneous, and required, especially in large networks. However, once a light path is established, the information can be transmitted quickly. Optical packet switching is a potential transport solution to close the gap between the electrical (IP/MPLS) layer and the optical (DWDM) layer. Messages are broken into small packets. The packets are transmitted over independent paths. There is no need to establish end-to-end paths. There is no need to reserve resources end to end.

This can avoid congestion and failures in the network. Resources are dynamically and locally assigned and released. Thus, packet switching has the ability to dynamically allocate network resources with fine granularity and with excellent scalability.

1.4 Roadblocks to Optical Packet Switching

It is beneficial to use packet switching rather than light path switching. However the packet switching needs to satisfy two requirements. The first requirement is to have transparency to packet size. The optical packet switching network needs be able to handle packets of varying sizes. The second requirement is to handle packet arriving asynchronously at high speed. Optical Packet switching needs optical buffers to store and forward packets. Large optical buffer is hard to come by. This limits input data rate and throughput. There is possible packet loss due to packet conflict and overflow of the buffer. There is a need to have conflict reduction and/or resolution schemes. The trend has been to use light paths with resource reservation in spite of the associated problems.

1.5 Recent Developments in Optical Memory Size and Processor Speed and their Impact on Optical Packet Switching

Some Recent developments have increased the feasibility of optical packet switching.

There are better optical buffers. Currently there is a reported available non-recirculating optical buffer with a size of 793 ns [5]. This optical buffer with a longer time delay will allow more time to find a route for an optical packet. There are improved high-speed processors for routing table look up. Currently available table look up rates is 213.4 Mlps for IPv6 packet with 128 bit addresses [6]. This is sufficient to satisfy high speed link OC-768 (40 Gbps) with 150000 routing entries. This faster routing table look up system will allow more routes for the optical packet to be looked up per unit time. There is a 5 GHz memory

read/write system [7]. This development will enable routing tables to be updated at a higher rate. There is high-speed optical switching. Wavelength division multiplexing/demultiplexing now has many channels. Dense wavelength division multiplexing can have up 320 channels.

1.6 Purpose of Dissertation

The purpose of the dissertation is to develop high speed optical packet switch using packet contention reduction and contention resolution techniques. The packet contention reduction and contention reduction techniques will be taking advantage of available higher speed processors and implementing a number of contention resolution methods in time (larger buffer size), wavelength (conversion), and space (Next Best Route). The contention resolution methods will be using dynamically updated Link & Channel Availability Table and dynamically updated hierarchical Routing Table (OSPF, Next Best Route). There will be many WDM channels available per fiber. Packets will be delayed rather than saving the full packet. Preambles will be added to reduce the delaying needed for data portion of packet.

Chapter 2 Optical Packet Switching

2.1 Background

2.1.1 High Level Architecture of an Optical Packet Switch

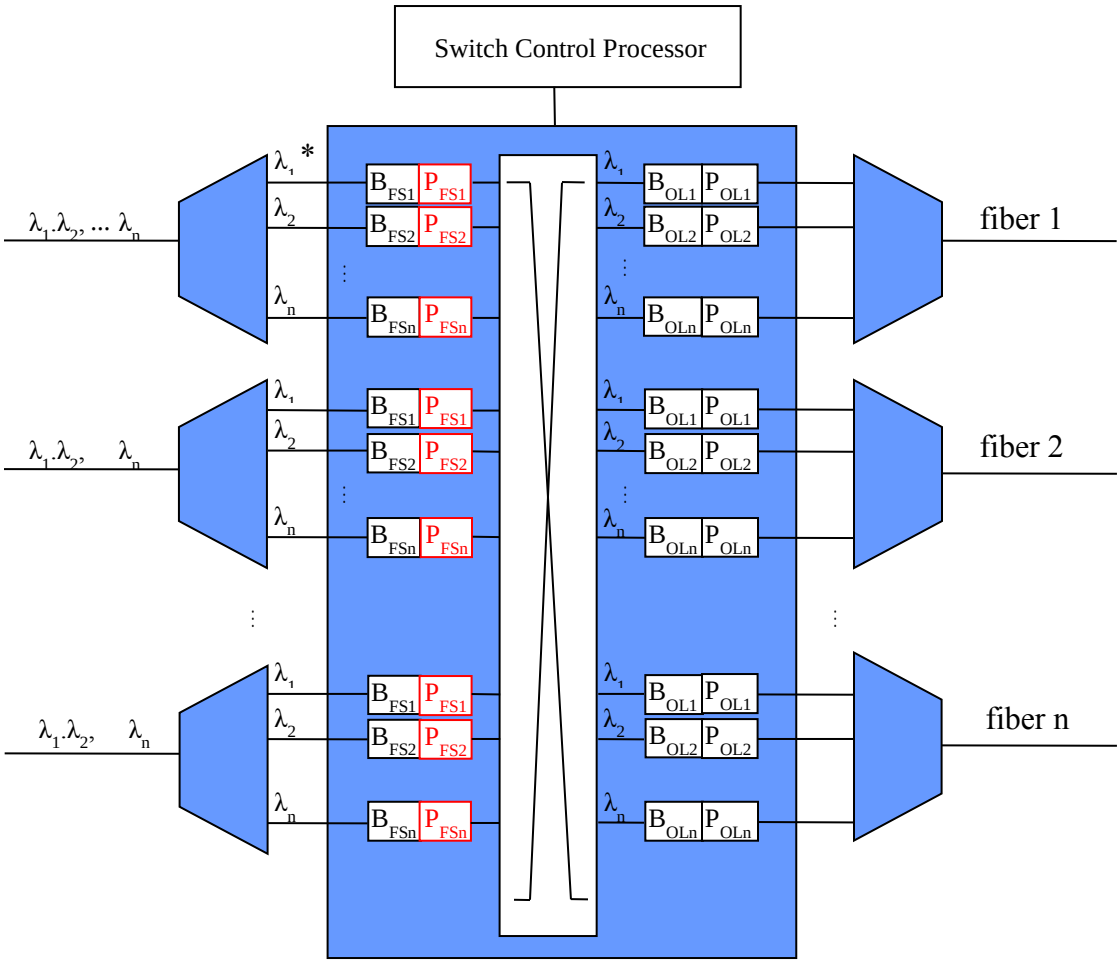

Figure 3 High Level Architecture of the Optical Packet Switch

The high level architecture of the optical packet switch is shown above in Figure 3. Packets are arriving at the demultiplexer on each input fiber. The demultiplexer separates the incoming packets into separate channels. Each input and output fiber contains N active

channels and M spare channels. The center frequency on the input side of the switch is denoted by λ^{i}_{kl} on the l-th channel on the k-th fiber. The center frequency on the output side of the switch is denoted by λ^{o}_{kl} on the l-th channel on the k-th fiber. The packet interarrival time is known. Each input channel has one forwarding buffer and one processor. When the packet arrives to the input buffer the packet header is separated and converted to electrical information. A route is found for the packet while the packet body is delayed optically in the buffer. Once a route is found for the packet, the switch is configured by the Switch Control Processor and a new label written just as the packet is leaving the optical buffer. The packet is forwarded to the output buffer. At the output buffer the packet label is removed and converted to electrical information. A route is found for the packet and a new label is written for the packet and attached the packet as the packet leaves the output buffer. The packet is then multiplexed with other channels in the multiplexer at the switch output and forwarded to the next switch.

2.1.2 High Level Operation of an Optical Switch

2.1.2.1 Input Side

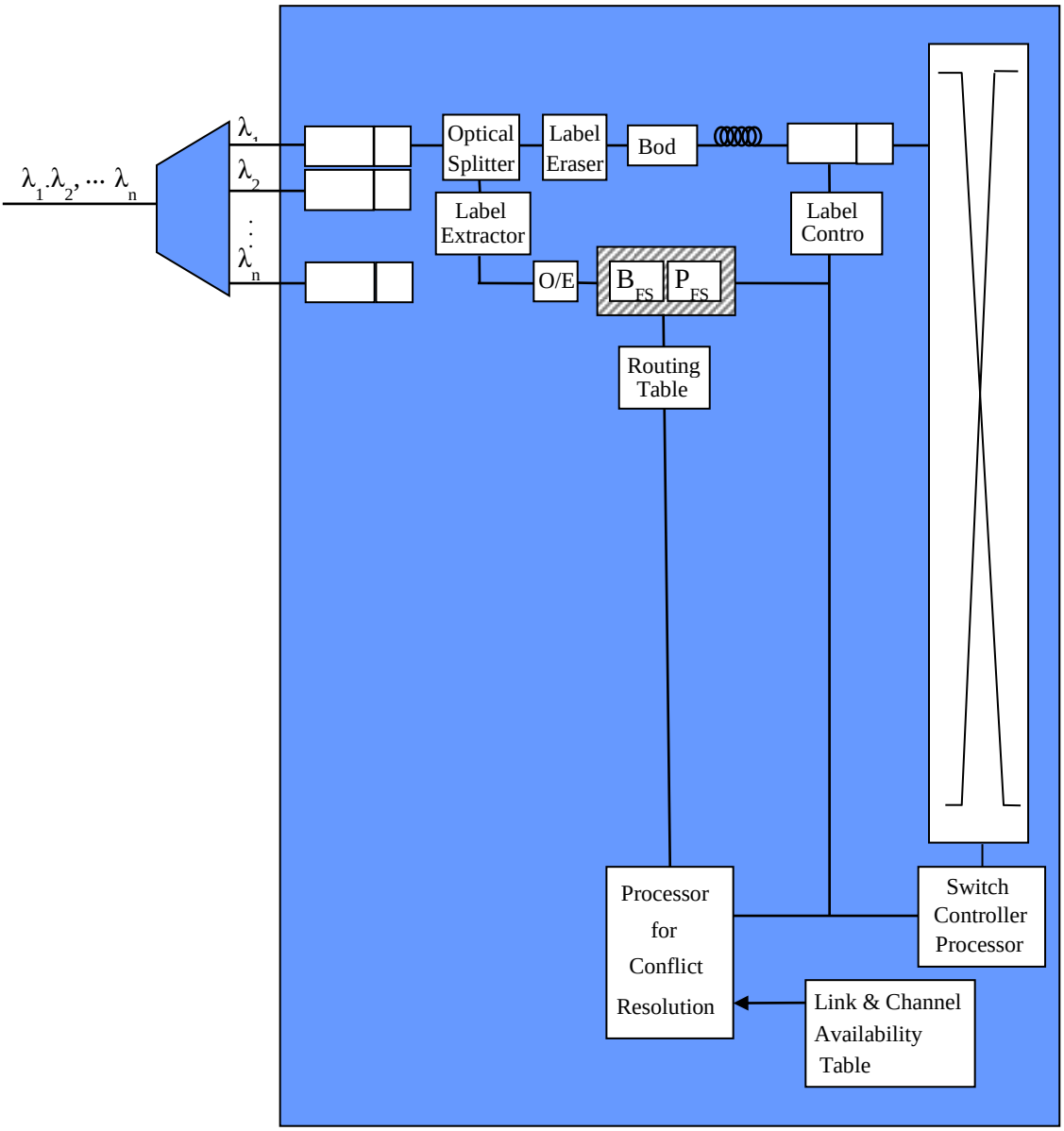

Figure 4 Detailed Operational Architecture of Input Side of an Optical Packet Switch

The detailed operational architecture of the input side of an optical packet switch is shown on the previous page in Figure 4. Packets arrive to the switch asynchronously at the switch's de-multiplexer. The packets are de-multiplexed and passed through an optical splitter. On one path from the optical splitter the label is erased from the packet and the packet is delayed in the optical buffer. On the other path from the optical splitter, the label is extracted from the packet. The label is then converted from optical information to electrical information in the O/E converter. The packet label is then sent to electrical buffer B_{FS}. The buffer's processor reads the packet header. The processor consults the routing table to find route for the packet. If a route cannot be found, the Processor for Conflict is consulted. The Processor for Conflict has route availability information from the Link and Channel Availability Table. Once a path is found, the revised packet label is sent to the label controller and the switch controller. The label controller generates an optical label when the packet exits the optical buffer. The switch controller sets up a path to an output buffer for the packet to be sent.

2.1.2.2 Output Side

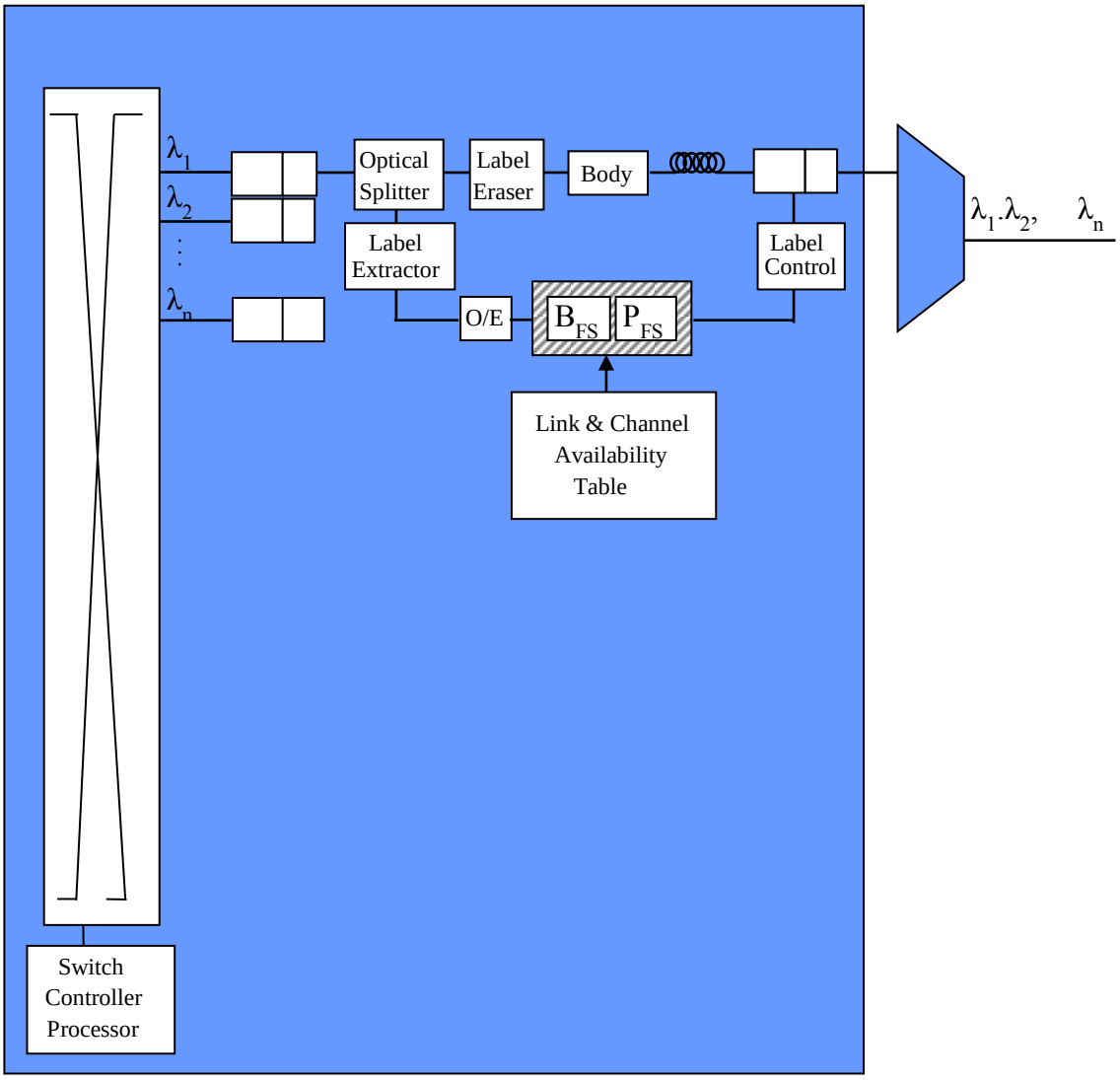

Figure 5 Detailed Operational Architecture of Output Side of an Optical Packet Switch

The detailed operational architecture of the output side of an optical packet switch is shown above in Figure 5. The optical packet arrives at the output fiber. The optical packet is passed through an optical splitter. On one path from the optical splitter the label is erased from the

packet and the packet is delayed in the optical buffer. On the other path from the optical splitter, the label is extracted from the packet. The label is then converted from optical information to electrical information. The packet label is then sent to electrical buffer B_{FS}. The buffer's processor compares the packet label with available routes. The processor consults the Link and Availability Table to find route for the packet. Once a path is found the revised packet label is sent to the label controller. The label controller generates an optical label when the packet exits the optical buffer. The optical packet is multiplexed with other packets and sent to its next hop.

2.1.3 Background

2.1.3.1 Previous Work on Packet Switching

2.1.3.1.1 Unified Study

The paper entitled, "A Unified Study of Contention-Resolution Schemes in Optical Packet-Switched Networks," presents a comprehensive study of contention-resolution schemes in an optical packet-switched network. The objective of the study is to provide a unified study of a network of optical routers. The study includes contention resolution in wavelength, time, and space dimensions. The study has three main areas. The first main area is how to accommodate all three dimensions of contention resolution in an integrated optical router. The second main area is how the performance of the three dimensions compares with each dimension. The final area is how various combinational schemes can be architected and how the combinational schemes perform. Simulation experiment results capture the characteristics of different contention-resolution schemes. The simulation results quantify the upper-bound average offered transmitter load for the simulated schemes [25].

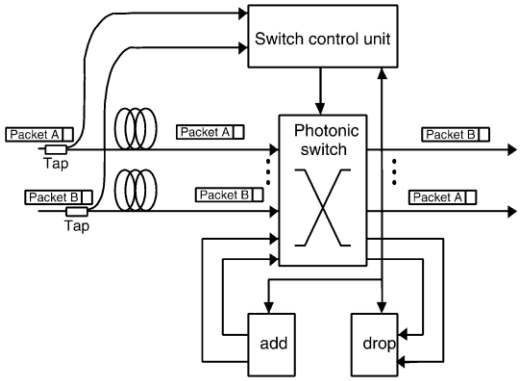

Figure 6 Unified Study's Node Architecture in an Unslotted Network [25]

Figure 6 to the left shows the general node architecture and packet behavior for unslotted networks in the Unified Study. The fixed-length fiber delay lines are used to hold the packet when the header is being processed and the switch fabric is configured to route the packet. All packets have the same amount of time delay with the same relative position in which they arrived, unless packet contention occurs. Each node has a number of add/drop ports. The number of drop/add ports will depend on the nodal degree. Each drop/add ports will correspond to multiple client interfaces reflecting multiple wavelengths on each fiber. Every input interface on the switches will be connected to a local receiver. Every output interface on the switches will be connected to a transmitter. Different contention-resolution schemes give lead to different architectures. The contention resolution schemes are wavelength conversion, single or multi-wavelength buffering, deflection, reservation of path ahead, no contention resolution, and delay for reservation [25].

Optical buffering utilizes one or more optical fiber delay lines to loop the signal from the output back to the input of the switch fabric. The study considers both single-wavelength and multi-wavelength optical buffering. The single-wavelength optical buffer is when the delay line can only take one packet at a time. The multiple-wavelength buffer is when each

delay line is terminated by a multiplexer and a de-multiplexer. A multiple-wavelength buffer can accommodate multiple packets on multiple wavelengths. When the multiple-wavelength buffer is compared with the single-wavelength buffer, the multiple-wavelength buffer requires a larger switch fabric and additional hardware such as multiplexer and de-multiplexer. The multiple-wavelength buffer achieves a larger capacity optical buffering on multiple wavelengths. The simulation results in the paper shows far improved performance for the multiple-wavelength delay lines [25].

In contention resolution utilizing wavelength conversion, the signal on each wavelength from the input fiber is first de-multiplexed and sent into the switch. The switch is capable of recognizing the contention and selecting a suitable wavelength converter leading to the desired output fiber. The wavelength converters can convert any incoming wavelength to a fixed desired wavelength or they can convert one or several pre-determined incoming wavelengths to a fixed desired wavelength. The paper reports that the majority of wavelength-conversion techniques demonstrated to date convert to one single wavelength channel. The paper cites a source that reports parametric wavelength conversion is a promising technique offering multichannel wavelength conversion without measurable crosstalk. The paper cites a second source that reports the conversion mechanism can scale well without a large number of wavelength converters by virtue of limited multichannel wavelength conversion [25].

Space deflection is used to resolve packet contention after time and wavelength conversion. Space deflection is carried out in hub nodes. Hub nodes are nodes that have higher nodal degree. The hub nodes will serve as major routing nodes. Individual nodes will have a deflection policy to deflect only to specific nodes. The deflection policy would only be deflected to a node that would eventually lead back to the original next hop [25].

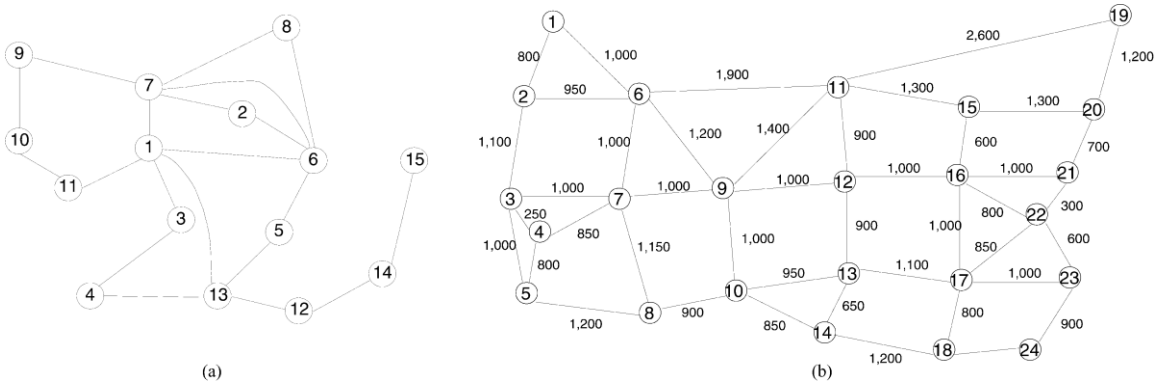

Figure 7 Unified Study's Topology 1 and Topology 2 [25]

Topology 1 and Topology 2 from the Unified Study is shown in Figure 7 above. Topology 1 represents a metro ring network. Topology 2 represents a WAN network. The link length in Topology 1 is 20 km. The link lengths in Topology 2 are shown in Figure 5. Each fiber modeled using 4, 8, and 16 wavelengths. The data rate for each fiber is 2.5 GBPS [25].

The study reports that the main characteristic of internet traffic is its self-similarity. The study also reports that it has been shown in the literature that self-similar traffic can be generated by multiplexing multiple sources of Pareto-distributed ON/OFF periods. The ON period would correspond to back to back packet trains. The OFF periods would be the time

where no packets would be transmitted. The study used a Hurst parameter of ON- and OFF-period duration distribution of 0.9. Packets arrive without any gap during the ON period [25].

The Unified study used a 19th order polynomial to reproduce the IP packet size distribution. The maximum size was set to be 1500 bytes. The probability distribution function was derived from a cited source. The probability function is shown below in Figure 8 [25].

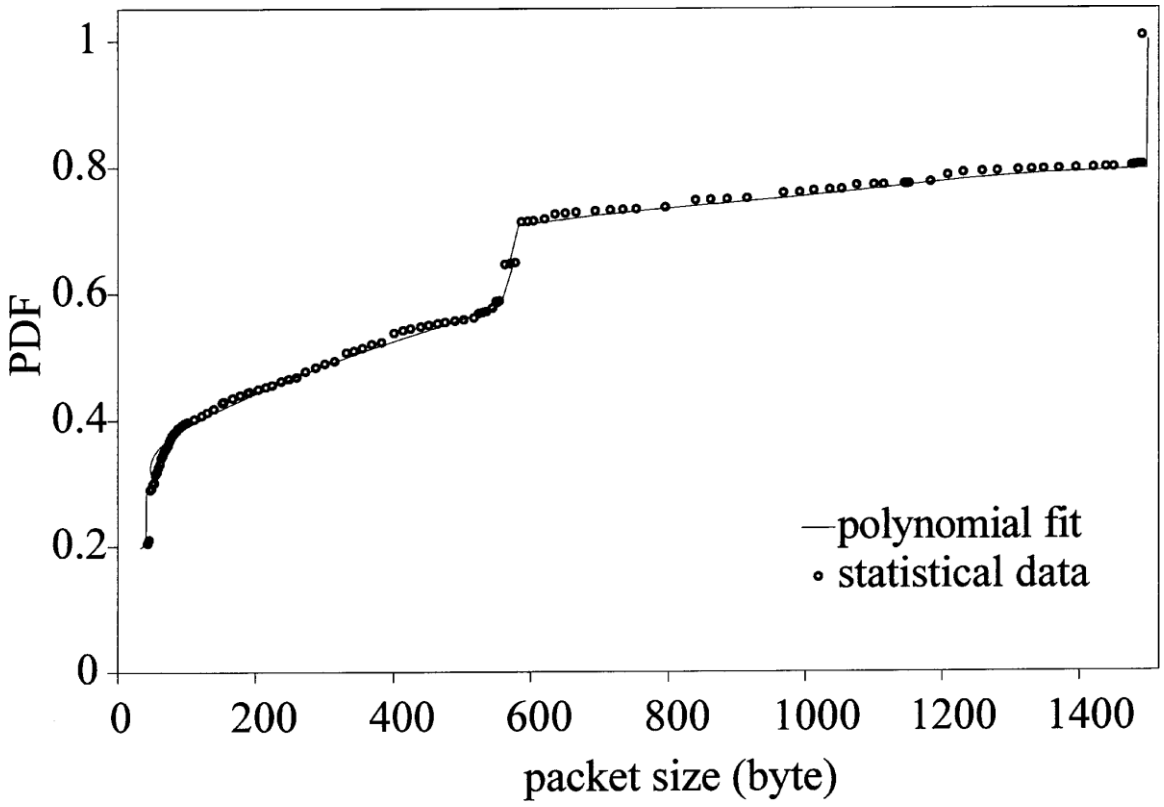

Figure 8 The Unified Probability Distribution Function of IP Packet Sizes [25].

There were three performance metrics chosen to evaluate network performance. The three performance metrics are network throughput, packet loss rate, and average hop distance. The packet loss rate is the total number of dropped packets divided by the total number of packets generated. The network throughput is defined by [25]

$$\text{Network throughput} = \frac{\text{total number of bits successfully delivered}}{\left(\frac{\text{network transmission capacity x simulation time}}{\text{ideal average hope distance}}\right)}$$

$$\text{Network transmission capacity} = (\text{total \# of links}) \times (\text{\# of wavelengths per link}) \times (\text{data rate})$$

The Unified study reports that network throughput is the fraction of the network resource that successfully delivers data. The Unified study reports the average hop distance as the hop distance a packet can travel, averaged over all the possible source destination pairs possible. The ideal average hop distance is 2.42 for Topology 1 and 2.99 for Topology 2 [25].

All the results from the Unified study are plotted with offered transmitter load as the abscissa. The offered transmitter load is the total number of bits offered per unit of time divided by the line speed. The average offered link load per wavelength is [25]

$$\text{Average offered link load} = \frac{\text{average offered TX load x total \# of TX x average hope distance}}{\text{\# of wavelengths x total number of uni-direcdtional links}}$$

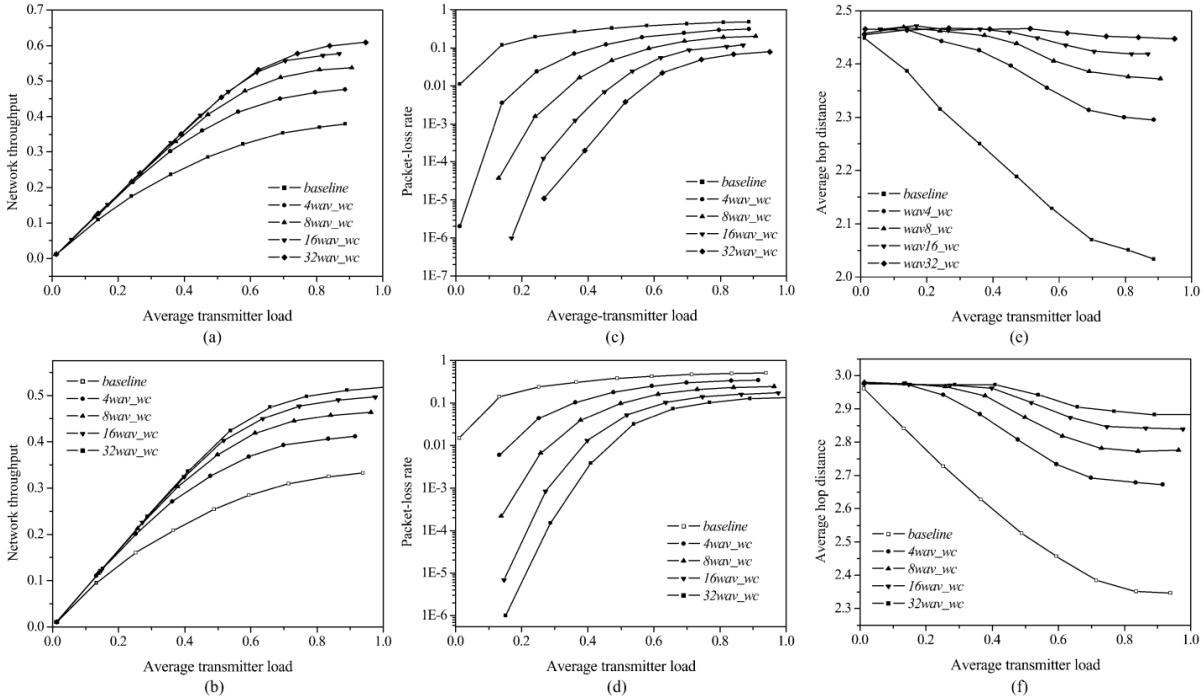

Figure 9 Wavelength Conversion Results for the Unified Study [25]

The wavelength conversion results for the Unified Study are shown above in Figure 9. The average transmitter load is normalized to 2.5 gigabits per second. Figure 9(a) shows the network throughput for wavelength conversion with different number of wavelengths for Topology 1. Figure 9(b) shows the network throughput for wavelength conversion with different number of wavelengths for Topology 2. The network throughput is normalized to 2.5 gigabits per second. Four wavelengths are simulated in baseline without wavelength conversion. The Unified Study reports that more wavelengths provide better throughput

performance. The margin of improvement decreases when the number of wavelengths increases. The network throughput for all architectures is too low. The recommended architectures provide higher throughput with a 10 gigabit per second line [25].

Figure 9(c) and 9(d) compares the packet loss rate for Topology 1 and Topology 2 respectively. Packet loss rates are reduced as the number of wavelengths increases. However, the packet loss rate for all architectures is too high. The recommended architectures in the dissertation provide much lower packet loss rates with a 10 gigabit per second line rate [25].

In the architectures using optical buffering, all the optical delay lines are 1 km in length. This represents a 5 microsecond delay. The delay line is long enough to hold 12000 bits.

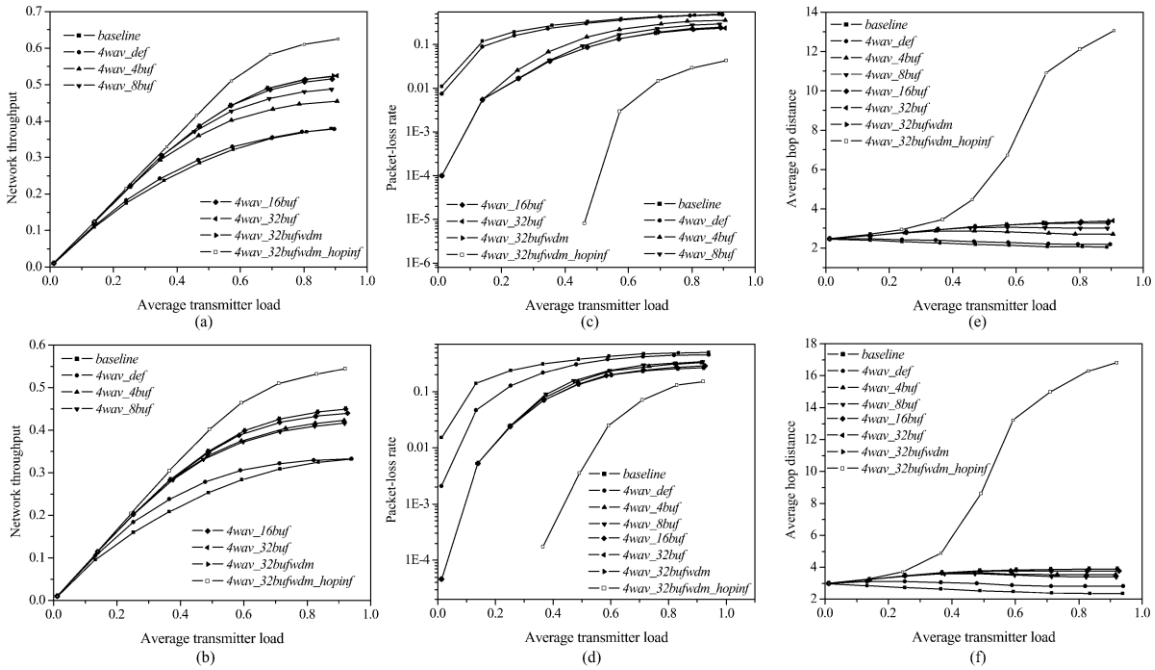

Figure 10 Unified Study's Results for Optical Buffering and Deflection [25]

Figure 10 shows the Unified Study's results for optical buffering and deflection. The average transmitter load is normalized to 2.5 gigabits per second. All architectures have four wavelengths with different buffering and deflection settings. Figure 9(a) compares the network throughput of different optical buffers and deflection architectures for Topology 1. Figure 9(b) compares the network throughput of different optical buffers and deflection architectures for Topology 2. The network throughput is normalized to 2.5 gigabits per second. Network throughput increases with the number of delay lines. The network throughput saturates after the number of delay lines reaches 16. The maximum hop count limits the number of times a packet can enter a delay line. This effected architectures with 32 delay lines. The maximum hop count was removed in the curves containing hopinf. The network throughput increased considerably in both cases. This improvement was

considerable less than the recommended architectures in the dissertation. The recommended architectures provide higher throughput with a 10 gigabit per second line [25].

Figure 10(c) and 10(d) compares the packet loss rate for Topology 1 and Topology 2 respectively. The average transmitter load is normalized to 2.5 gigabits per second. The Unified study observes that deflection in Topology 2 provides a lower packet loss rate than in Topology 1. The Unified study explains that difference by stating state Topology 2 is a more densely connected network. However, the packet loss rates for all architectures are much higher than the recommended architectures in the dissertation. The recommended architectures in the dissertation provide much lower packet loss rates with a 10 gigabit per second line rate. The recommended architectures provide higher throughput with a 10 gigabit per second line [25].

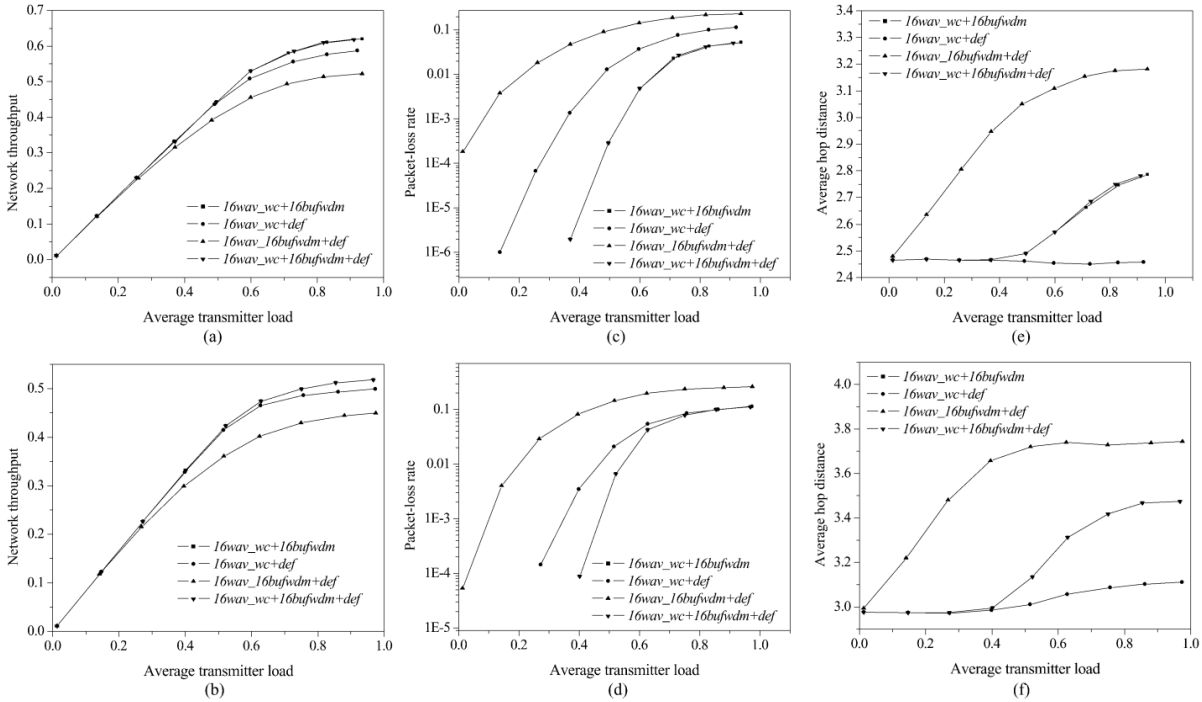

Figure 11 Unified Study Results for Combinational Architectures [25]

Figure 11 shows the Unified Study's results for combinational architectures for wavelength conversion, optical buffering, and deflection. The average transmitter load is normalized to 2.5 gigabits per second. All architectures have sixteen wavelengths with different buffering and deflection settings. Figure 11(a) compares the network throughput of different optical buffers and deflection architectures for Topology 1. Figure 10(b) compares the network throughput of different optical buffers and deflection architectures for Topology 2. The network throughput is normalized to 2.5 gigabits per second. The architecture that uses all three dimensions of wavelength, time, and space has the best network throughput. The Unified Study observes that when wavelength conversion and buffering are used, deflection provides little change in performance. The network throughput for all architectures is too

low. The recommended architectures provide higher throughput with a 10 gigabit per second line [25].

Figure 11(c) and 11(d) compares the packet loss rate for Topology 1 and Topology 2 respectively. The average transmitter load is normalized to 2.5 gigabits per second. The wavelength conversion combined with buffering and deflection provided the best performance. The packet loss rate on the best performer is too high and the network throughput is too low. The recommended architectures in the dissertation provide much lower packet loss rates with a 10 gigabit per second line rate [25].

2.1.3.1.2 All-Optical Contention Resolution with Prioritization

The paper entitled, "160 Gb/s All-Optical Contention Resolution with Prioritization using Integrated Photonics Components," presents a method for 160 Gb/s all-optical contention resolution with prioritization using integrated photonic devices. The paper discusses the functional diagram of the all-optical contention resolution method, the experimental set-up, and the results of the experiment [26].

Figure 12 below shows the functional diagram of the optical circuit capable of resolving contention in wavelength and space domain between packets at the same wavelength [26].

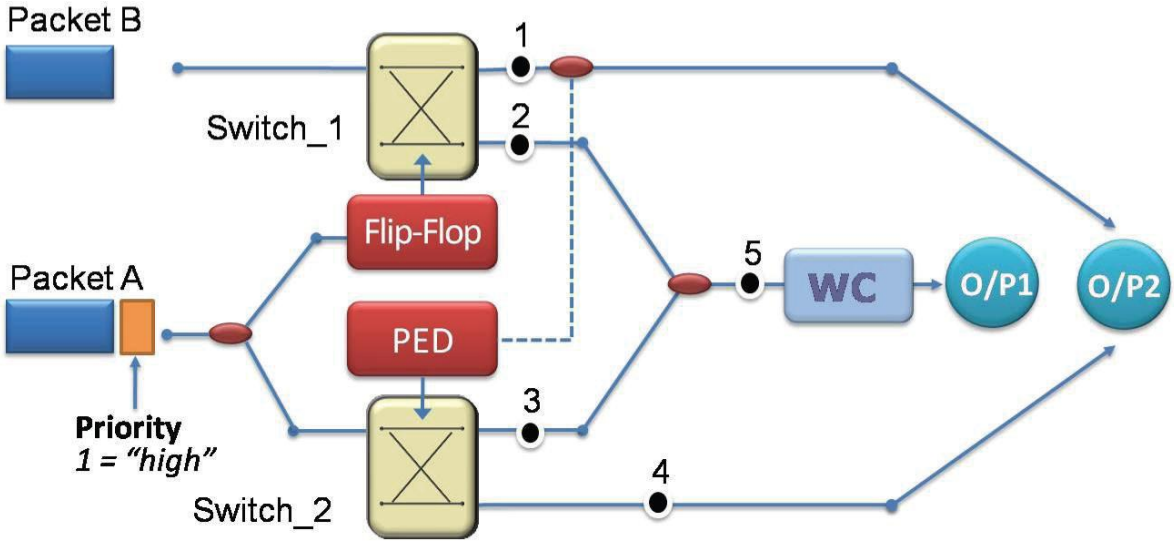

Figure 12 Functional Diagram for All-Optical Contention Resolution Method [26]

The functional diagram consists of two 1x2 switches (Switch_1 and Switch_2), an Optical Flip-Flop (OFF), a Packet Envelope Detection circuit (PED), and a 160 Gb/s all-optical wavelength converter (WC). Packet A enters the all-optical circuit from input 1. Packet A's priority flag is extracted using narrowband filtering. The extracted label is sent to the Flip-Flop (OFF). This is to generate an optical pulse at λ_3 with length slight higher than the data packets. The optical pulse is used to control the state of Switch_1 and route Packet B. In the presence of λ_3, packet A has priority. Packet B is transmitted from output_2 of Switch_1. The packet is then routed to O/P1. O/P1 is a contention port. In the absence of λ_3, packet B is transmitted from output_1 and the main output port O/P2. Packets leaving output_1 of Switch_1 are optically split to the PED. The PED circuit generates packet envelope signals at λ_4. Switch_2 is controlled by the PED output. Packet A is routed to output_1 of Switch 2

and transmitted to O/P1 when the PED is on. The PED is on when packet B exits and packet A has low priority. If packet A has priority, then it is sent to output_2 of Switch_2 and out O/P2. Output_1 of Switch_1 and output_2 of Switch_2 are combined to the main output port O/P2. Output_2 of Switch_1 and output 1 of Switch_2 are combined to point 5 to resolve contention in the space domain. Packets at point 5 that are wavelength converted to λ_5 are represented as contention resolution in the wavelength domain [26].

The experimental setup for the 160 Gb/s all-optical contention resolution is shown below in Figure 13 [26].

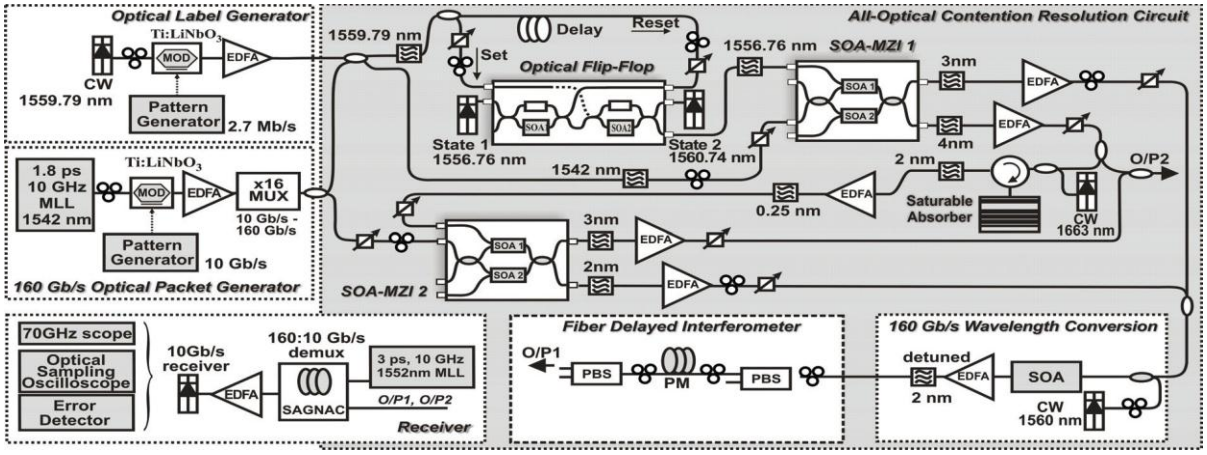

Figure 13 Experimental Setup for 160 Gb/s All-Optical Contention Resolution [26]

A 10 GHz mode-locked laser produced 1.8 picosecond (ps) pulses. The pulses were modulated into data packets containing a 2^7-1 psudorandom binary sequence (PRBS) pattern. The laser generated signal was rate multiplexed to 160 Gb/s in a fiber multiplexer. The laser generated signal produced a sequence of three packets with a 52 ns duration followed by an

empty packet slot. The signal was split in to two parts to create the two incoming packet streams. This is to provide two input streams. The priority flag was added to packet stream A and delayed 90 ns in relation to packet stream B. The priority flag was produced in a second modulator with a1.6 ns duration. Using an optical filter, packet stream A was separated from the priority flag. The extracted priority flag was optically split into two paths with one path being delayed 60 ns. This is to provide the Set and Reset signal to the OFF. The OFF produced 60 ns pulses with 1.4 decibels (db) variation. The optical path of Output_1 of Switch_1 led to the PED circuit. The PED circuit consisted of a passive slow absorber-based vertical-cavity semiconductor gate that can be saturated that is powered by a 1564 CW laser. Output_1 of Switch_1 and output_2 of Switch_2 were time synchronized and combined at the main output port O/P2. Output_2 of Switch_1 and output_1 of Switch_2 were also time synchronized and combined at the contention port O/P1. The contention output was combined with a 1560 CW laser. The light path circuit was directed on to the SOA and initiating the wavelength conversion. The SOA consists of a 1.1 mm long SOA with a 1.5 nm filter on the end and a delay interferometer. The two 160 Gb/s streams were demultiplexed to 10 Gb/s. The Bit Error Rate (BER) was evaluated for the two 10 Gb/s channels. The results are shown on the next page in Figure 14 [26].

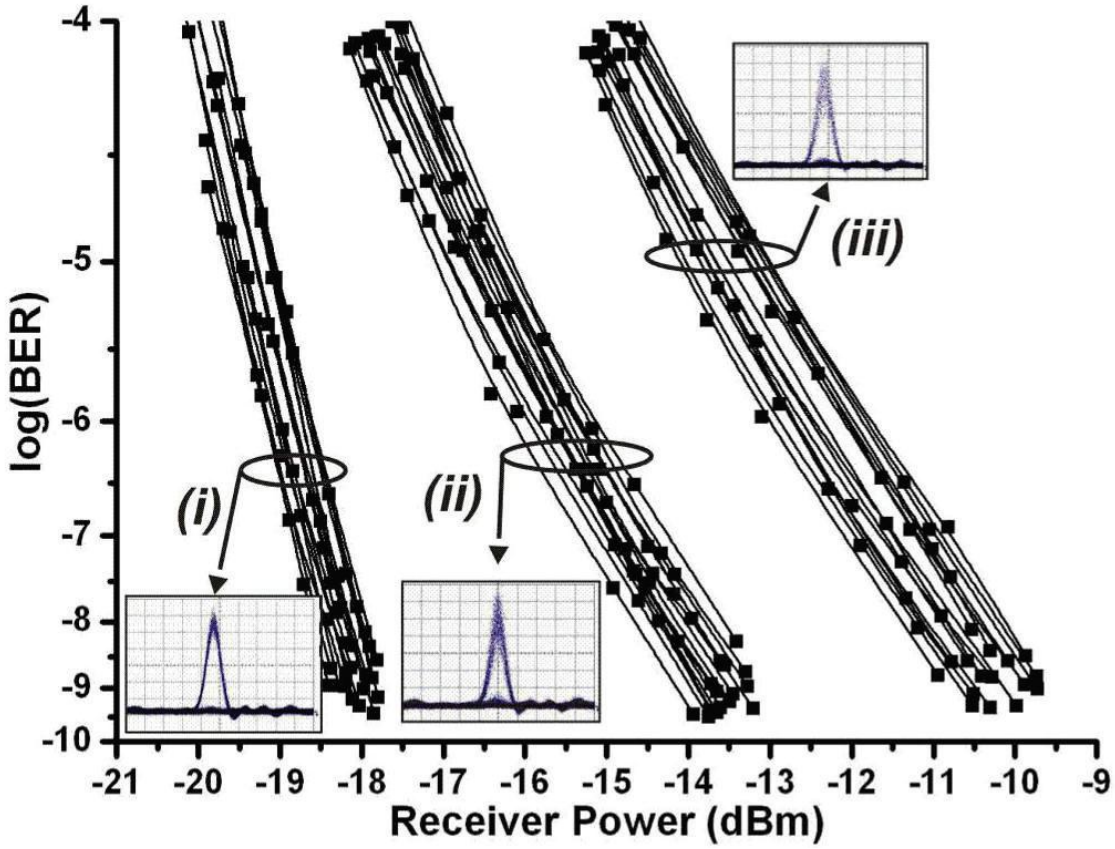

Figure 14 BER Performance for 160 Gbps Contention Resolution Scheme [26]

The contention resolution scheme in [26] provides a much higher line rate than the line rate in the dissertation. However the contention resolution scheme in [26] is limited to two input lines. This will not work in optical networks where there are many input and output lines. The dissertation will work with many input and output lines.

Chapter 3 Optical Packet Switch Developed in this Dissertation

3.1 High Level Architecture of a Packet Switch

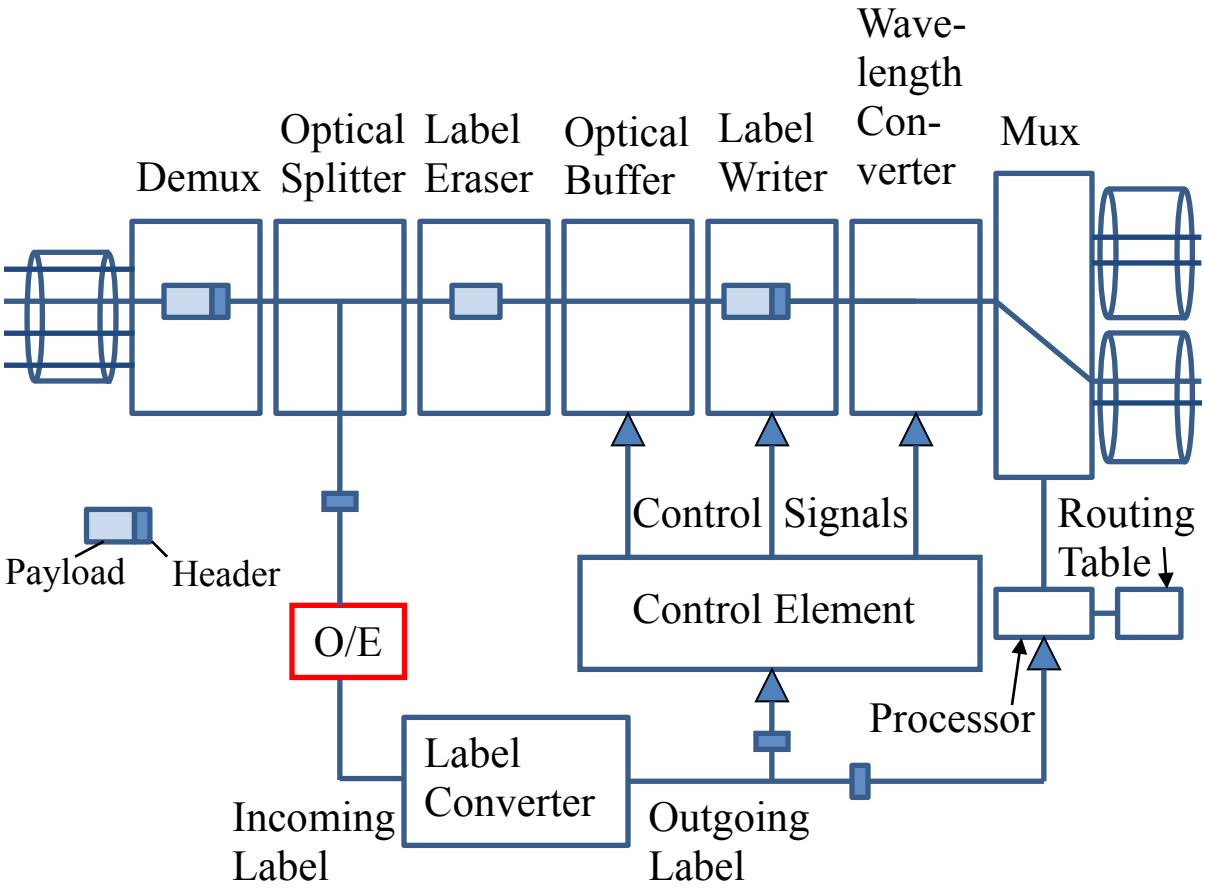

Figure 15 High Level Architecture for Optical Packet Switch [1]

The high level architecture for an optical packet switch is shown above in Figure 12. The high level architecture for an optical packet switch contains components which the optical packet is forwarded. The main components in which the optical packet is forwarded are the demux, the optical splitter, label eraser, optical buffer, wavelength converter, and mux. The packet arrives in the demux. Demux is short for demultiplexer. The packet contains the

header and the payload or body. The header has the packet's label. The body can have either user traffic or control traffic. The demultiplexer separates the wavelengths into separate paths. The optical splitter sends the packet to the control element and the label eraser. The label eraser extracts the header from the packet. The packet is sent to the optical buffer. The body of optical packet remains optical buffer while the packet header is being processed. The header is sent to the optical to electrical converter. The label is converted to electrical information, so the label can be processed electrically. The label is sent to the label converter. The label converter sends the label to the processor. The processor compares the label value to the routing table. Once the next hop is found the new label information is sent is sent to the label converter. The label converter sends the new information to the control element. The control element signals the label writer to write a new label. If the packet needs to be wavelength converted to resolve packet contention, the packet is wavelength converted. The packet is then sent to the mux. Mux is short for multiplexer. The packet is then sent to the requested wavelength and fiber [1].

3.2 Current Developments in Enabling Technology for Use in Theses

3.2.1 Larger Optical Memory

Optical memory is still limited. However optical memory has improved. Reported in [13] is a non-recirculating optical buffer using a crosspoint switch with a total buffer time of 793 nanoseconds. The crosspoint optical switch used in the optical buffer consists of two

waveguide layers. At each crosspoint of the switch two active vertical couplers (AVC) are formed by having an active waveguide stacked on top of both input and output passive waveguides. Switching is performed in the crosspoint by using carrier-induced refractive index and gain changes in the AVCs. The crosspoint ON state has the effective refractive index of the active upper layer reduced by the presence of injected carriers to equal that of the lower waveguide thereby allowing coupling. Gain is provided for the signal by the injected carriers in the active layer. This results in a high ON/OFF contrast.

4x4 Crosspoint switch fabrics were demonstrated. The switch fabrics are scalable without the inherent losses associated with broadcast and select schemes. A reference in [13] has shown that the crosspoint switch output power can be dynamically controlled on a packet to packet basis for a large input power range. Another reference in [13] is cited for having optical gain differences of less than 3 decibels (dB) are attainable between the shortest and longest switch paths. A reference in [13] is cited for having attained multicasting without optical split loss. Another reference is cited in [13] that achieves ultra-low OFF state crosstalk in the crosspoint switch by using the highly absorptive state of the active waveguide and the weakened coupling that attenuates the stray signal. The crosstalk is as low as –60 dB has been routinely demonstrated in [13]. The low crosstalk with ultra-fast switching speed, the crosspoint switch provides an excellent electro-optic switch fabric to be used in the implementation of optical packet switches in optical networks.

Additional information on optical delay lines can be found in [14]-[19].

3.2.2 Faster Processing Speed

A routing lookup system with routing application-specific integrated circuit (ASIC) and off-chip routing table for IPv6 is proposed in [20]. The off-chip routing table is a two-level hierarchical memory architecture memory architecture. The off-chip routing table is designed according to the prefix length distribution of 6Net router's routing table. 6Net was a three-year European project to demonstrate continued growth of the internet can be met using IPv6 as the Internet Protocol. The first level of off-chip routing table contains 91.89 percent of routing table entries. The ASIC is made of a content-addressable memory (CAM) and a function unit. The CAM is used as cache memory. The CAM has 1024 entries and guarantees an 80 percent hit ratio by first in first out (FIFO) replacement strategy. The proposed routing system lookup system has table look up rates of 28169 Mlps for IPv6 packet with 128 bit addresses. It is sufficient to satisfy high speed link OC-768 (40 Gbps). The routing table memory size is only 20.04 kilobytes (KB) using ternary content-addressable memory (TCAM), 10.24 KB using binary content addressable memory (BCAM), and 29.29 KB random access memory (RAM) for 1500 entries. In summary, the CAM with 1024 entries can guarantee an 80 percent hit ratio. The routing lookup speed can approach 213.4Mlps. The routing lookup speed satisfies the requirement of OC-768 [20].

In [21] an InGaP/GaAs heterojunction bipolar transitor (HBT) integrated circuit implementing a 64-bit programmable look up table (LUT) memory was developed, fabricated and evaluated. In order to demonstrate the high-speed memory application, a

mature and readily available InGaP/GaAs HBT technology was selected. A read function fast enough for a clock rate of 10 GHz was demonstrated by a simulation. An output eye diagram of the memory was generated as simulated at 5 GHz using Cadence's SPECTRE tools and including estimated parasitic capacitances. The circuit model was driven by a pseudo-random source. The circuit model determines a repeating random address set. The memory was synchronously toggled from read and write modes at various times during the transient simulation. Vertical markers on the eye diagram are used to measure the worst-case time delay from the sense amplifier's output to the rowdriver's output. This is the most critical delay path on the chip. The latency during a read cycle is marked with vertical markers on the eye diagram. The worst-case read cycle is 22 picoseconds (ps). The worst-case write cycle is 52 ps. The worst-case read cycle and worst-case write cycle result suggests that the circuit will be able to run in read mode at the target clock frequency of 10GHz. The GaAs HBT integrated circuit was packaged in a 32-pin multi-lead frame package. The 64-bit look up table (LUT) uses 2.0 millimeters (mm) x 2.0 mm of chip area. This includes output buffers but not bondpads. The chip contains approximately 500 transistors, and dissipates approximately 6 Watts (W) at -5.2 volts (V). Functionality of the integrated circuit is demonstrated with a digital test sequence that validates all memory states using an Agilent 16500B mainframe pattern generator and logic analyzer up to 100MHz. A pattern representative of a 27 pseudorandom binary sequence (PRBS) is first written to the memory. After the PRBS is written to memory, the same sequence is read out of the memory. Data in the memory was successfully held over a 30 minute period. A clock rate of

5 GHz was demonstrated experimentally. An Anritsu 12.5Gbps pseudo-random pattern generator source was used in high speed tests. After low-speed programming, a sequence of l's and O's were used to toggle the look up table (LUT) between two memory cells holding different bit values. The results demonstrate successful read operation up to 5GHz. In summary, an InGaP/GaAs HBT implementation of a 64-bit programmable LUT is demonstrated by simulation up to 1OGHz and validated experimentally up to 5GHz [21].

3.2.3 Numerous Wavelength Division Multiplexing Channels

Assume many channels. It is possible to have up to 320 channels per fiber. Hence, we can have an available channel all the time. There will be no blockage due to lack of wavelengths [1]-[4].

3.2.4 Network Processors

Network processors are programmable integrated circuits that perform specific applications. Applications that are typically used by network processors are traffic management, routing, and packet processing. Network processors are found in network routers and switches. Additional information can be found on specific network processors in [22] – [24].

3.2.4 Link and Channel Availability Table

Outgoing Link	Channel Type	Channel Number	Available
1	Active	1	Yes/No
	Active	2	Yes/No
	Active	3	Yes/No
		.	
		.	
		.	
	Active	N	Yes/No
	Spare	N+1	Yes/No
	Spare	N+2	Yes/No
		.	
		.	
		.	
	Spare	M+N	
Outgoing Link	Channel Type	Channel Number	Available
2	Active	1	Yes/No
	Active	2	Yes/No
	Active	3	Yes/No
		.	
		.	
		.	
	Active	N	Yes/No
	Spare	N+1	Yes/No
	Spare	N+2	Yes/No
	Spare	N+3	Yes/No
		.	
		.	
		.	
	Spare	N+M	
		.	
		.	
		.	
Outgoing Link	Channel Type	Channel Number	Available
L	Active	1	Yes/No
	Active	2	Yes/No
	Active	3	Yes/No
		.	
		.	
		.	
	Active	N	Yes/No

Spare	N+1	Yes/No
Spare	N+2	Yes/No
Spare	N+3	Yes/No
	.	
	.	
	.	

Table 1 Link and Channel Availability Table for Outgoing Links

The Link and Channel Availability Channels table is shown on page 33 in Table 1. The table shows the channel availability for each channel on outgoing links. Each outgoing link contains active channels and spare channels. Active channels transmit optical packets where possible and without packet drops. Spare channels transmit packets that would be dropped by the active channels because of packet contention.

3.3 Detailed Operational Architecture of Input Side of an Optical Packet Switch

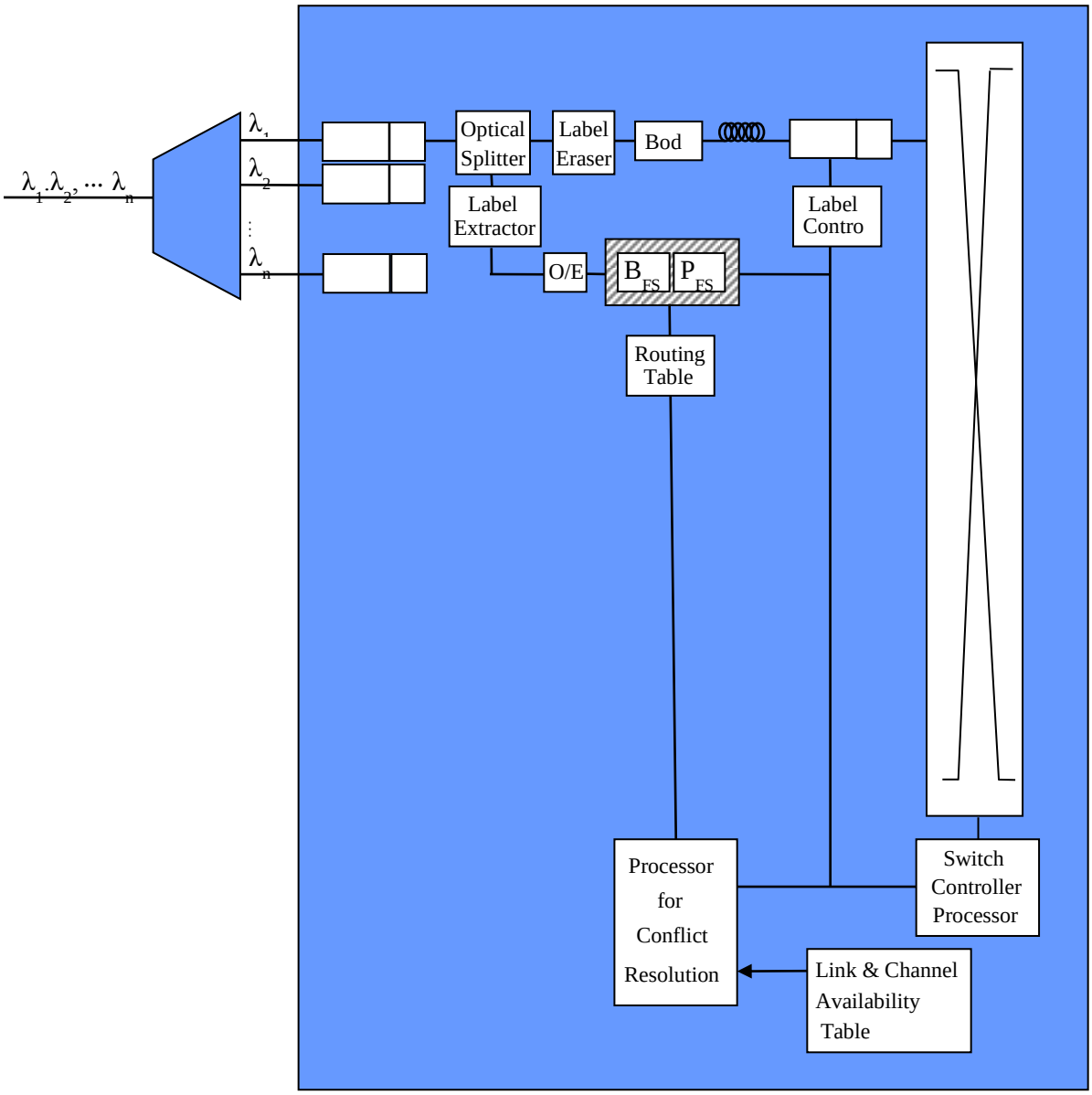

Figure 16 Detailed Operational Architecture of Input Side of an Optical Packet Switch

The detailed operational architecture of the input side of an optical packet switch is shown on the previous page in Figure 16. Figure 16 is described in Section 2.1.2.1.

3.4 Optical Packet Switch Operational Algorithm at the Switch Input

The steps for the optical packet switch operation algorithm at the input side of the optical packet switch are as follows for a packet arriving on the i-th incoming link:

1. The packet header is separated from the body of packet.
2. The main body of packet goes through the input optical buffer.
3. The packet header is processed electronically.
4. The destination node is determined.
5. The best outgoing link for this destination is determined by using the routing table.
6. The channel number k and the corresponding center frequency λ at which the packet arrived is determined.
7. It is determined whether the k-th channel or a spare channel on the best outgoing link is available by using the Link and Channel Availability (CA) Table.

8a. If a channel is available, then transfer the packet to the best outgoing link through the switching fabric using the switch control processor.

8b. If no acceptable channel is available on the best outgoing link then consult routing table and find the Next Best Route for the destination node of the packet and transmit the packet.

3.5 Flow Diagram of Algorithm of Optical Packet Switch Operation at the Switch Input

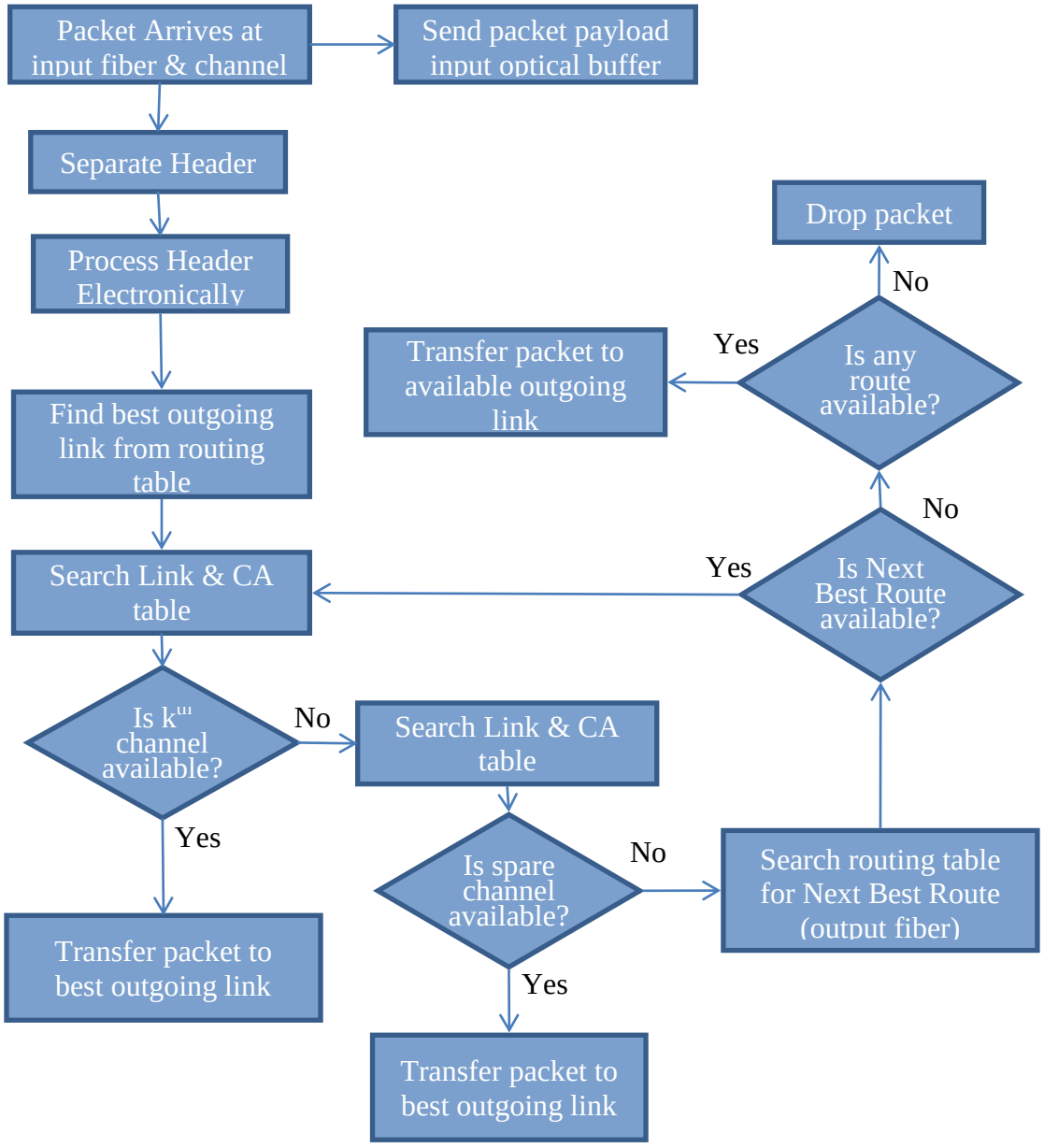

Figure 17 Flow Diagram of Algorithm of Optical Packet Switch Operation at the Switch Input

The flow diagram of algorithm of optical packet switch operation at the switch input is shown on the previous page in Figure 17.

3.6 Optical Packet Switch Operation at the Switch Output

The steps for the optical packet switch operation at the output of the switch are as follows:

1. If the k-th channel is available on the outgoing link on which the packet was transferred then transmit the packet.
2. If the k-th channel is not available on the outgoing link to which the packet was transferred, then find a spare channel on this link, convert the wavelength, and transmit the packet on this spare channel.
3. If no next best fiber and channel is available, send the packet on any available fiber and channel (Deflection).
4. If no fiber and channel is available, then drop the packet.

3.7 Flow Diagram of Algorithm of Optical Packet Switch Operation at the Switch Output

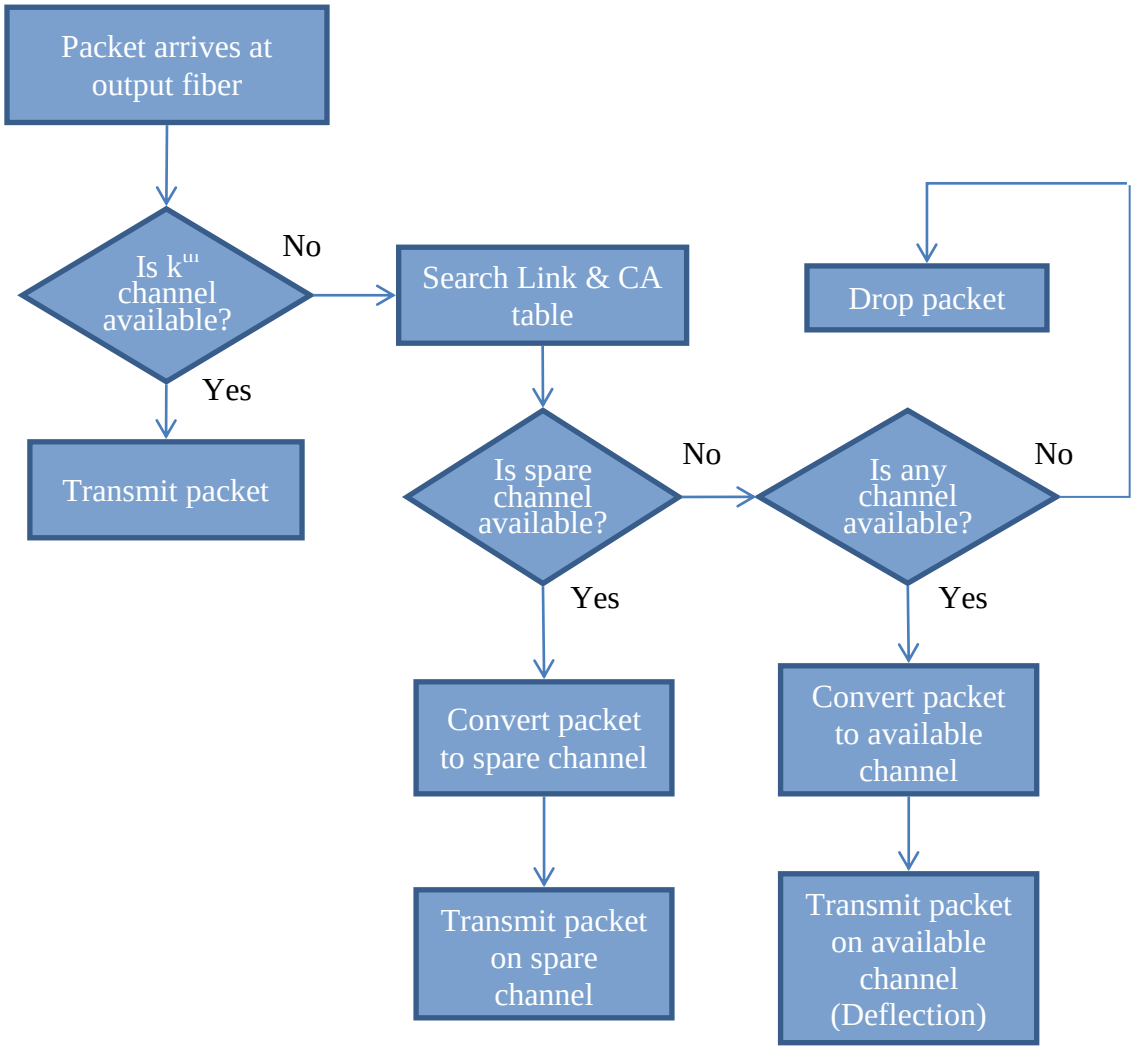

Figure 18 Flow Diagram of Algorithm of Optical Packet Switch

The flow diagram of algorithm of optical packet switch operation at the switch output is shown above in Figure 18.

3.8 Performance Evaluation

3.8.1 Introduction

The performance is evaluated in terms of packet loss rate, average throughput and total throughput. The Unified Study evaluated performance in terms of packet loss rate and network throughput.

3.8.2 Packet Loss Rate

The packet-loss rate is the total number of dropped packets divided by the total number of packets received at the switch.

3.8.3 Average Throughput per Line

The average throughput per line is the average of each line throughput. The throughput of each line is the average number of bits successfully transmitted by each output buffer per unit time, in bits per second.

Wavelength conversion and Next Best Route (NBR) reduce the average throughput per line. The amount of reduction to the average throughput per line is proportional to the number of lines that are used for wavelength conversion or Next Best Route.

3.8.4 Total Throughput

The total throughput is the sum of each line's average throughput.

3.8.5 Network Throughput

Network throughput as defined by [25] is the fraction of the network resource that successfully delivers data. When packets are dropped, a part of the network capacity is not utilized in transferring the bits that are dropped.

$$\text{Network throughput} = \frac{\text{total number of bits successfully delivered}}{\left(\frac{\text{network transmission capacity x simulation time}}{\text{ideal average hope distance}}\right)}$$

Network transmission capacity

= (total # of links) x (# of wavelengths per link) x (data rate)

Chapter 4 Simulation Models of the Optical Packet Switch

A number of architectures were simulated in OPNET Modeler. The list of architectures is shown below in Table 2.

4.1 List of Architectures Modeled, Simulated and Evaluated

#	Architectures Scenarios Modeled, Simulated and Evaluated
1	Baseline (Single Input & Output Processor, no wavelength conversion, no Next Best Route)
2	Single Input Processor (no contention resolution)
3	Single Input Processor with Next Best Route
4	Single Input Processor with 4 Wavelength Conversion
5	Single Input Processor with 3 Wavelength Conversion
6	Single Input Processor with 2 Wavelength Conversion
7	Single Input Processor with 1 Wavelength Conversion
8	Parallel Input Processor
9	Parallel Input Processor with 1 Wavelength Conversion
10	Parallel Input Processor with 2 Wavelength Conversion
11	Parallel Input Processor with 3 Wavelength Conversion
12	Parallel Input Processor with 4 Wavelength Conversion
13	Parallel Input Processor with Next Best Route

Table 2 List of Architectures Modeled, Simulated and Evaluated

All architectures except the baseline architecture have multiple (one per wavelength) output processors. Each processor has a processing speed of 10 Gbps.

4.2 Optical Packet Switch Architectures

4.2.1 Introduction

The simulation consists of several parts like forwarding buffers, output buffers, source models, and destination models. Each part is shown in Figures 19 through Figure 22.

4.2.1.1 Forwarding Buffers

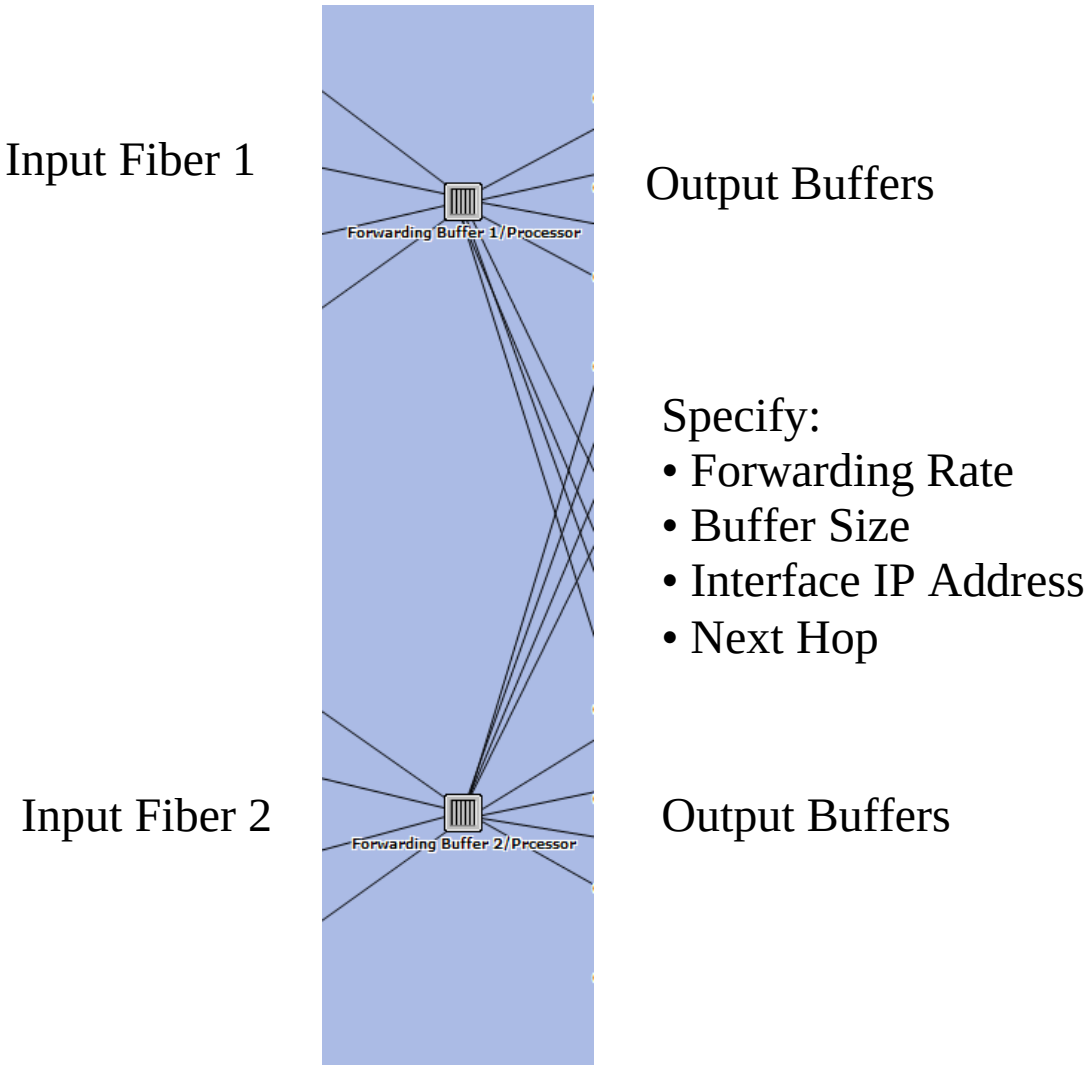

Figure 19 Graphical Representation of Forwarding Buffers in OPNET Modeler

The graphical representation of forwarding buffers in OPNET Modeler is shown in Figure 19 above. Forwarding buffers delay the optical packet while the optical packet header is

processed. In the simulations the forwarding rate, buffer size, interface IP address, and next hop were specified.

4.2.1.2 Output Buffers

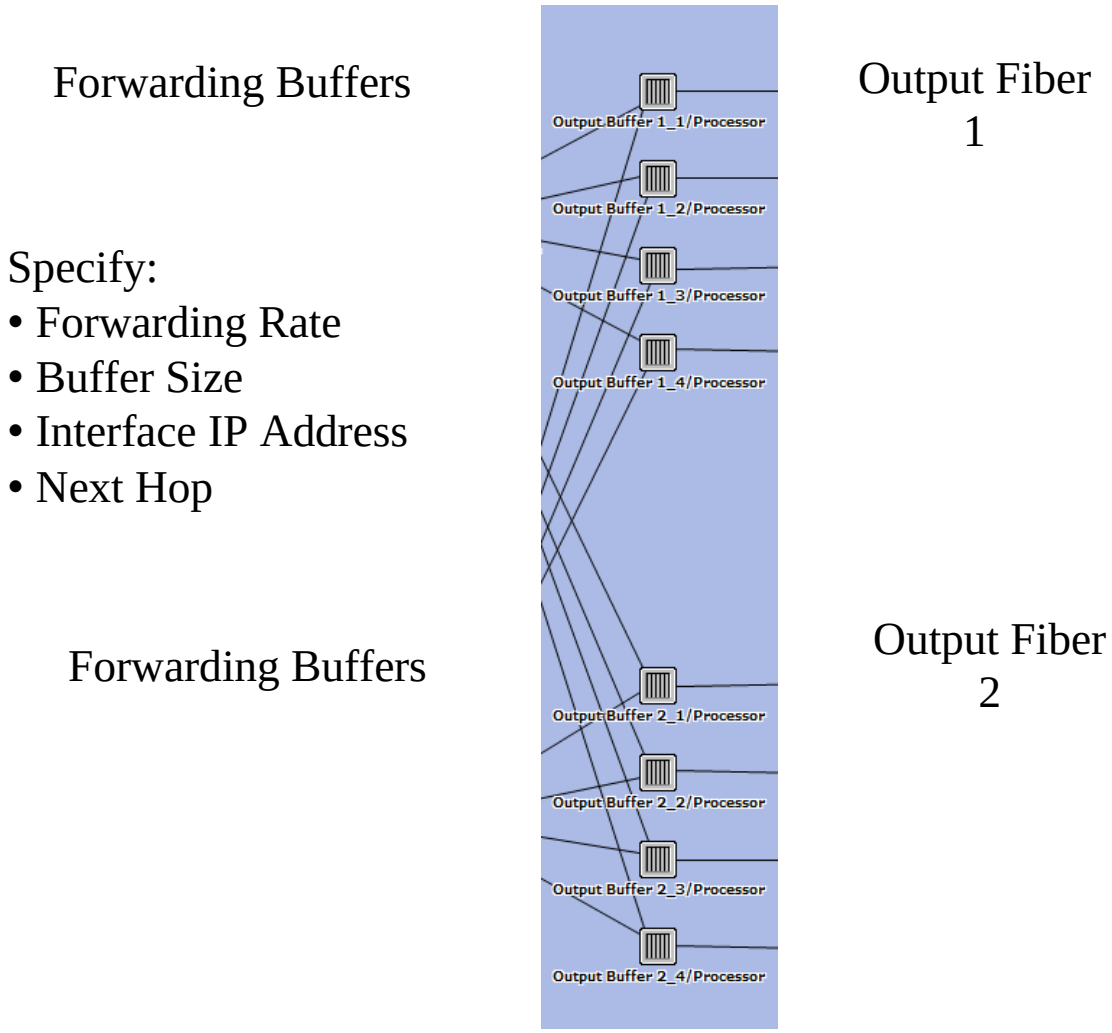

Figure 20 Graphical Representation of Output Buffers in OPNET Modeler

The graphical representation of output buffers in OPNET Modeler is shown in Figure 20 above. Output buffers delay the optical packet. In the simulations the forwarding rate, buffer size, interface IP address, and next hop were specified.

4.2.1.3 Source Models

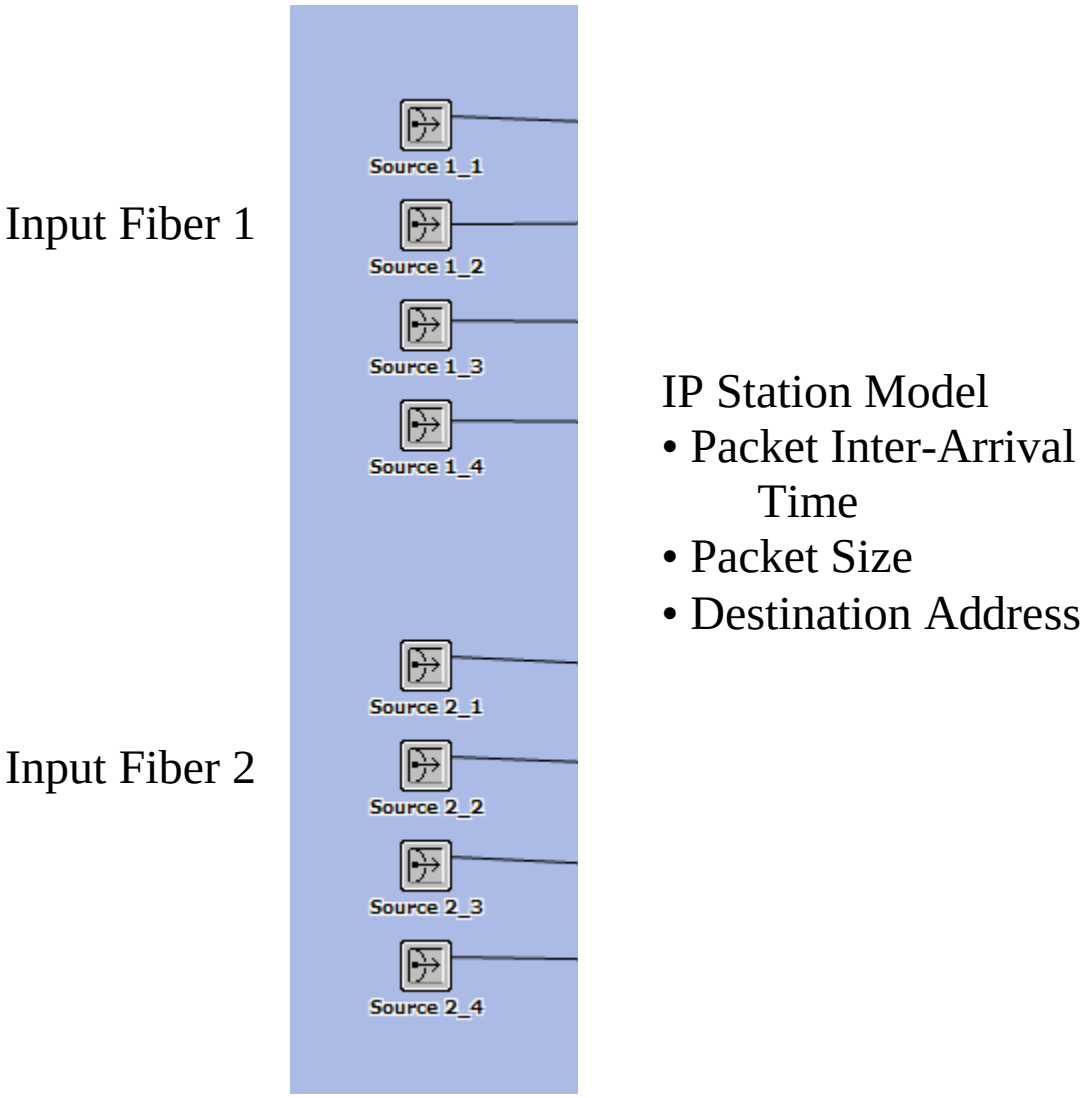

Figure 21 Graphical Representation of Source Models in OPNET Modeler

The graphical representation of source models in OPNET Modeler is shown in Figure 21 above. Source models generate packets in the simulations. In the simulations, the packet inter-arrival time, packet size, and destination IP address were specified.

4.2.1.4 Destination Models

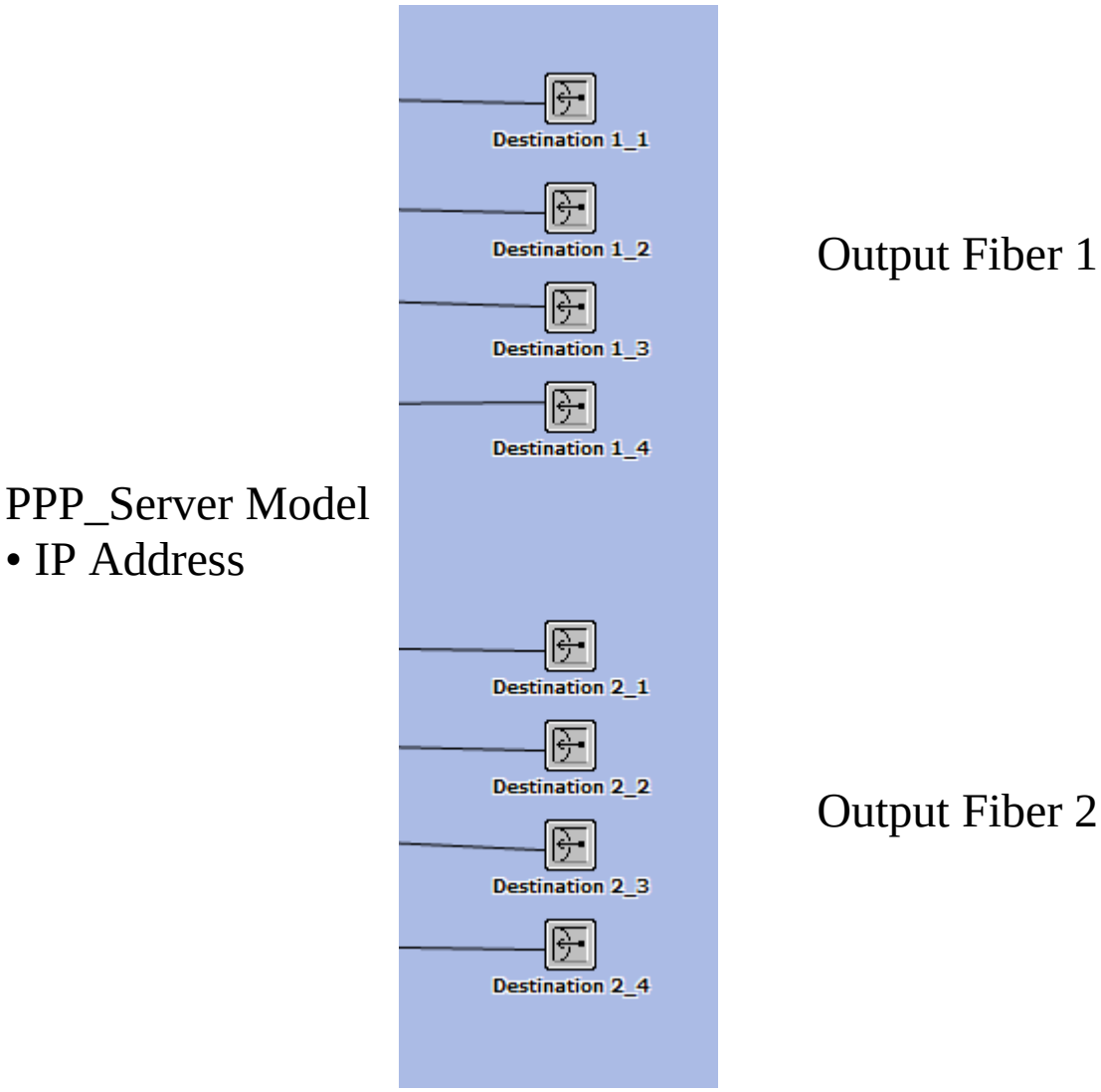

Figure 22 Graphical Representation of Destination Models in OPNET Modeler

The graphical representation of destination models in OPNET Modeler is shown in Figure 22 above. Source models generate packets in the simulations. In the simulations, the packet inter-arrival time, packet size, and destination IP address were specified.

4.2.1.6 Single Input Processor Configuration

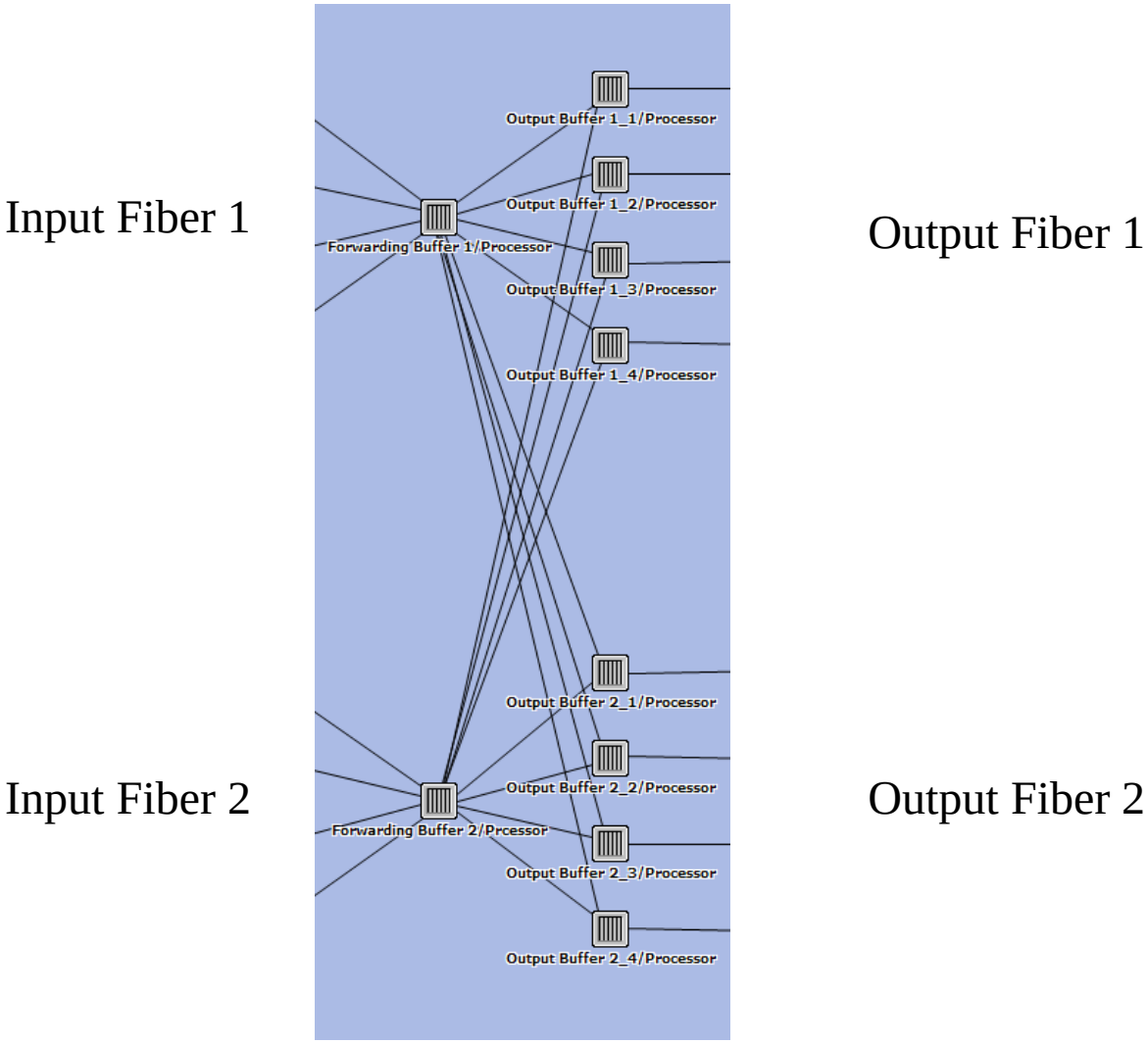

Figure 23 Single Input Processor Configuration

The graphical representation of the Single Input Processor configuration is shown in Figure 23. The simulation model uses the Single Input Processor configuration for simulations.

4.2.1.7 Parallel Input Processors Configuration

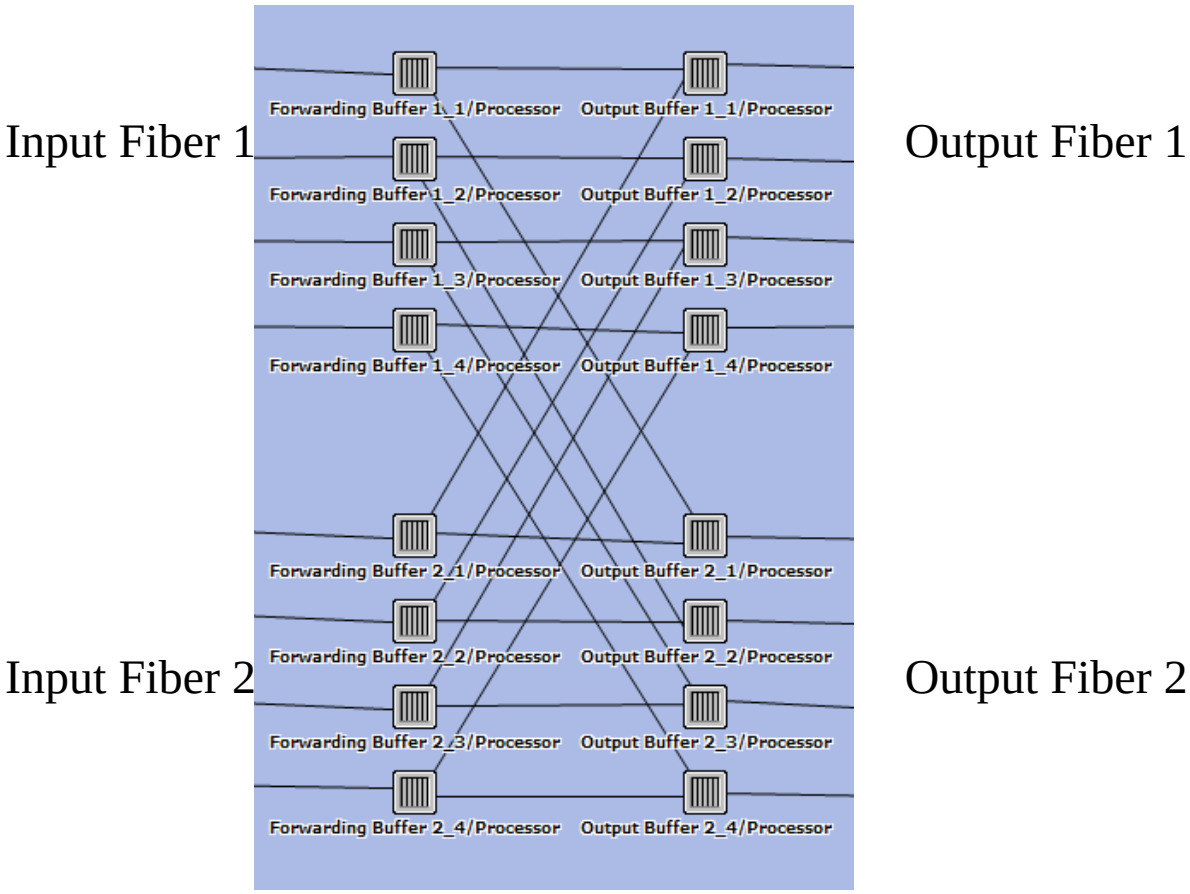

Figure 24 Parallel Input Processor Configuration

The graphical representation of the Parallel Input Processor configuration is shown in Figure 24. The simulation model uses the Parallel Input Processor configuration for simulations.

4.2.1.5 Routing within the Switch

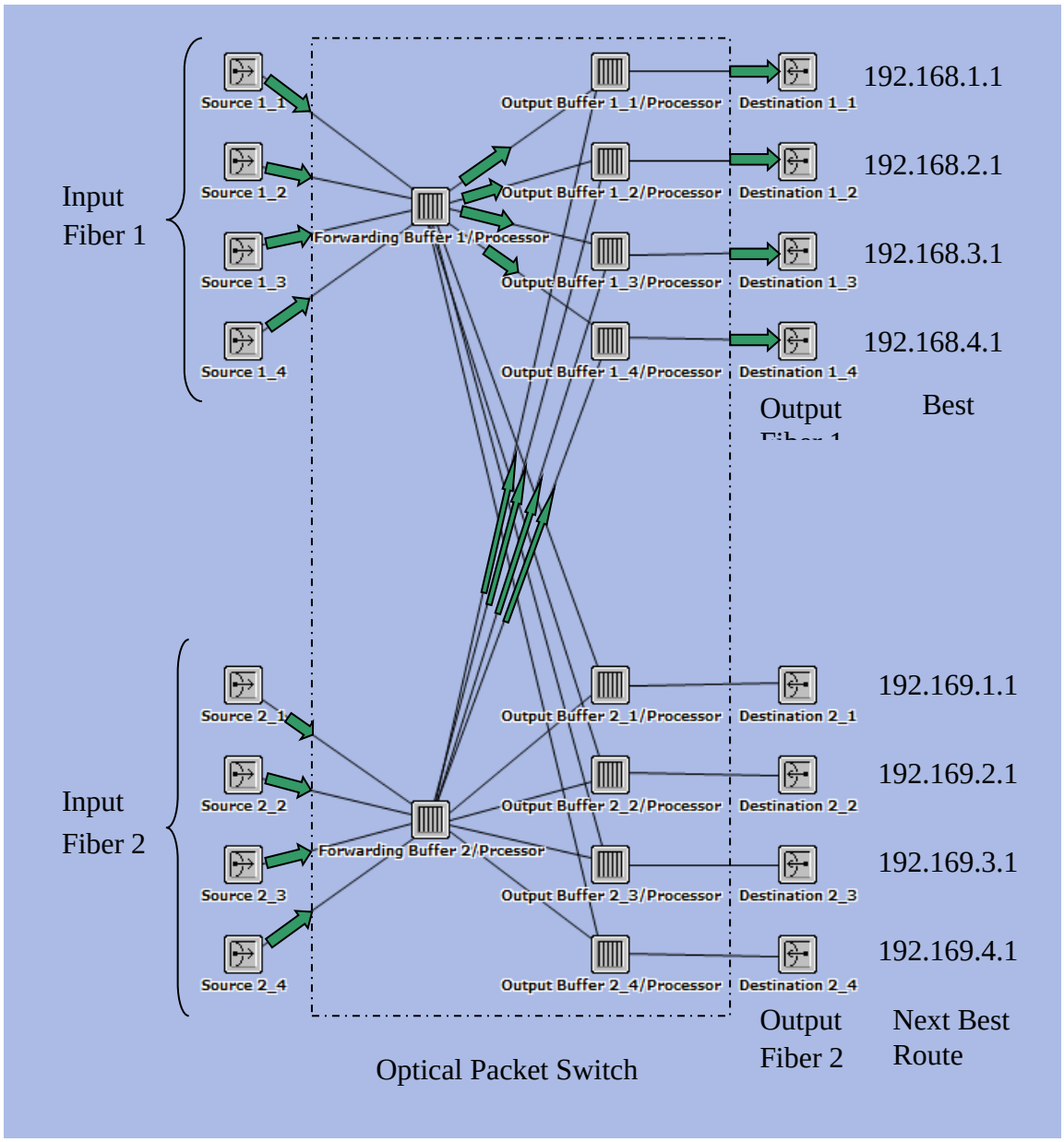

Figure 25 Routing Operation within Optical Packet Switch Model

The routing within the optical packet switch was performed by setting up static routes at the forwarding buffer and the output buffer. IP addresses were assigned at each destination. The next hop on the routing table was specified based on the destination IP address. A graphical illustration of the routing operation with the optical packet switch is shown on the previous page in Figure 25.

Chapter 5 Traffic Flows and Switch Architectures

5.1 Baseline Architecture

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. The Baseline scenario has one forwarding buffer and one output line buffers per fiber. Each forwarding buffer has one processor that forwards packets at 10 gigabits per second. Each output buffer also has one processor that forwards packets at 10 gigabits per second. Each fiber has four wavelengths. The switch architecture and the traffic flow for the Baseline architecture is shown in Figure 26 on the next page. The traffic flow is represented by the arrows.

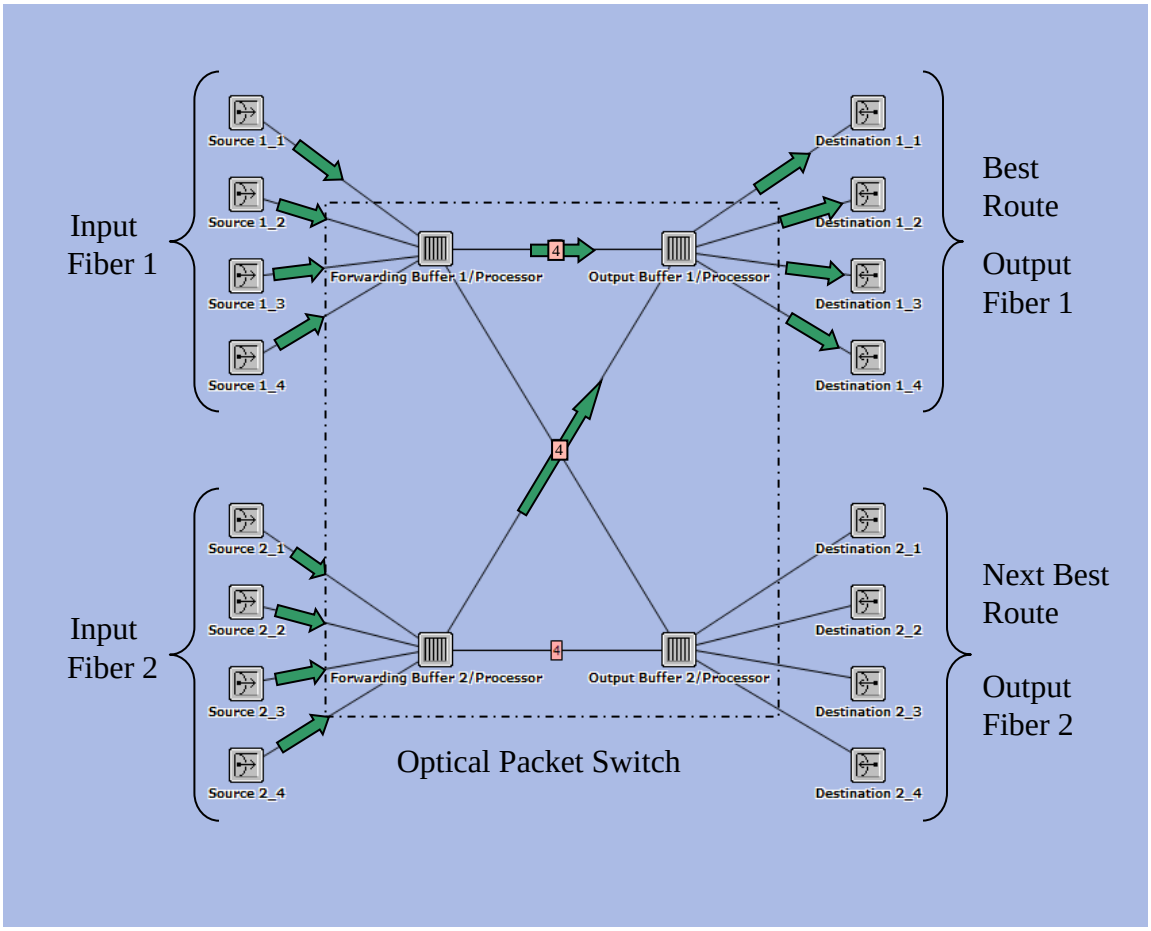

Figure 26 Switch Architecture and Traffic Flow for Baseline Architecture

5.2 Single Input Processor Architecture

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. The Single Processor Baseline scenario has one forwarding buffer and four output line buffers per fiber. Each forwarding buffer has one processor that forwards packets at 10 gigabits per second. Each output buffer also has one processor that forwards packets at 10 gigabits per second. Each fiber has four wavelengths. The switch architecture and the traffic flow for the Single Input Processor architecture is shown in Figure 27 on the next page. The traffic flow is represented by the arrows.

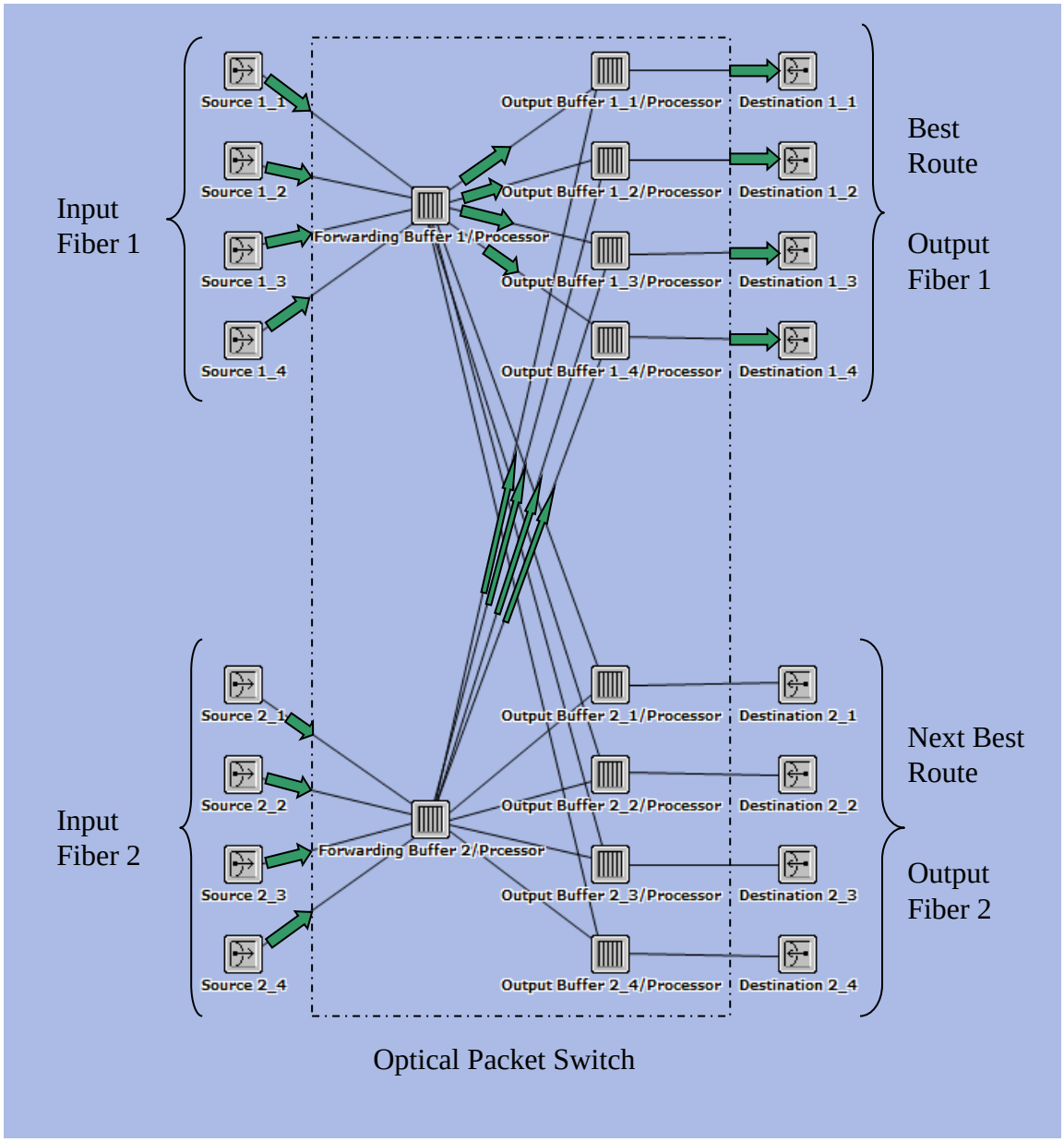

Figure 27 Switch Architecture and Traffic Flow for Single Input Processor Architecture

Each input fiber has four sources generating traffic. There is one source per wavelength. All packets generated by the sources are a constant 1500 bytes. All traffic from input Fiber 1 is sent to Output Fiber 1 on the same wavelength. All traffic from Input Fiber 2 is sent to

Output Fiber 2. There is one destination per wavelength. Each destination contains a traffic receiver and a traffic sink. There is no wavelength conversion on any packets. All traffic remains on its original wavelength. Traffic is being generated for one second in all simulation runs. Simulations were run for traffics being generated on each wavelength for 0.1, 2, 4, 6, 8, and 10 gigabits per second.

5.3 Single Input Processor Architecture with Next Best Route

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. Each source generates 1500 byte packets. The Single Input Processor with Next Best Route architecture has one forwarding buffer and four output line buffers per fiber. Each forwarding buffer has one processor that forwards packets at 10 gigabits per second. Each output buffer also has one processor that forwards packets at 10 gigabits per second. Each fiber has four wavelengths. The switch architecture and the traffic flow for the Single Input Processor Architecture with Next Best Route is shown in Figure 28 on the next page. The traffic flow is represented by the arrows.

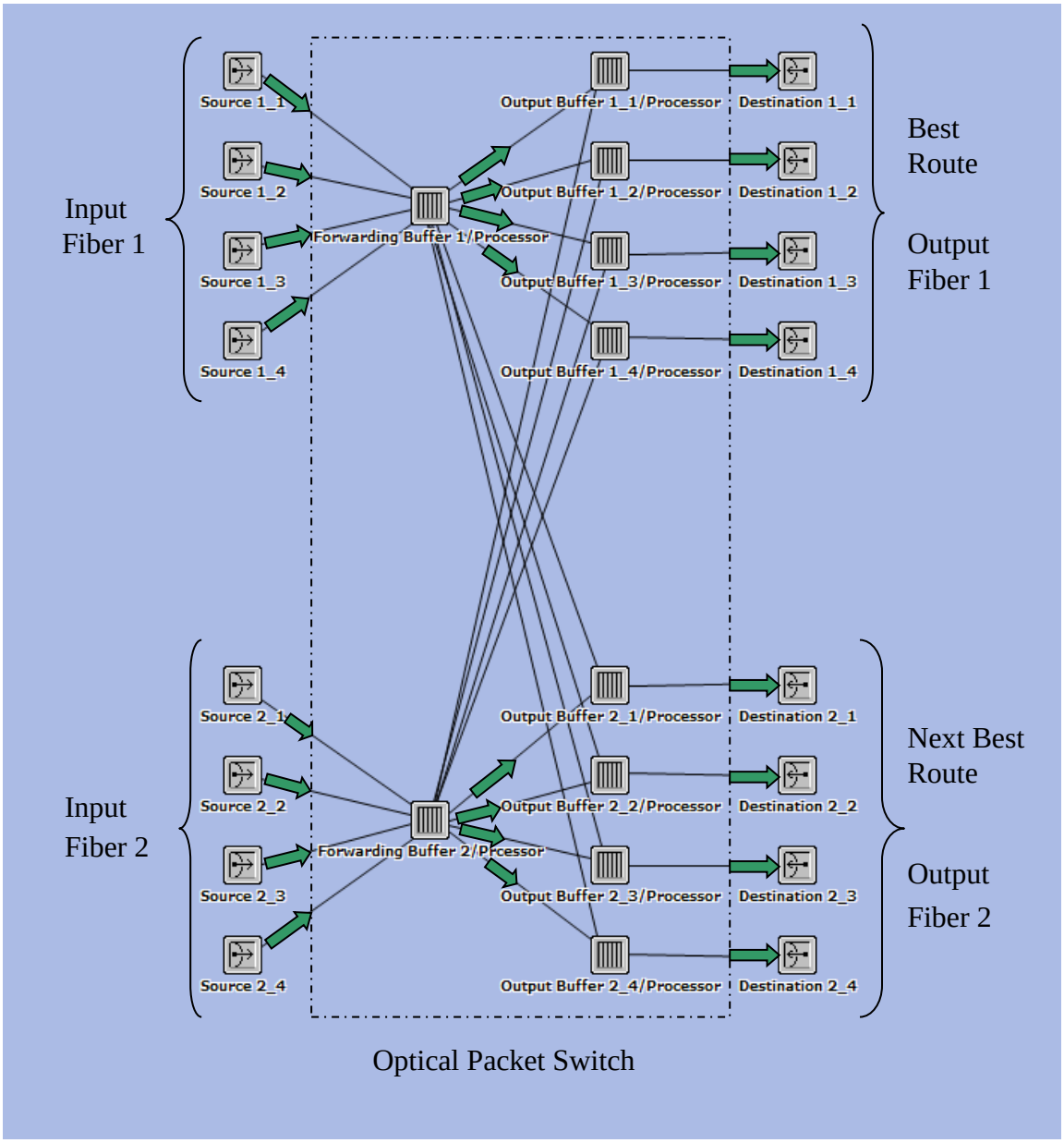

Figure 28 Switch Architecture and Traffic Flow for Single Input Processor Architecture with Next Best Route

Each input fiber has four sources generating traffic. There is one source per wavelength. All packets generated by the sources are a constant 1500 bytes. All traffic from Input Fiber 1

is sent to Output Fiber 1. All traffic from input Fiber 2 is normally sent to Output Fiber 1 but is sent to Output Fiber 2. There is one destination per wavelength. Each destination contains a traffic receiver and a traffic sink. There is no wavelength conversion on any packets. All traffic remains on its original wavelength. Traffic is being generated for one second in all simulation runs. Simulations were run for traffics being generated on each wavelength for 0.1, 2, 4, 6, 8, and 10 gigabits per second.

5.4 Single Input Processor Architecture with Four Wavelength Conversion

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. Each source generates 1500 byte packets. The Single Processor with WC4 scenario has one forwarding buffer and one output buffer per fiber. Each forwarding buffer has one processor that forwards packets at 10 gigabits per second. Each output buffer also has one processor that forwards packets at 10 gigabits per second. Each fiber has four wavelengths. All traffic from Input Fiber 1 is sent to Output Fiber 1 on the same wavelength. The traffic on Fiber 2 is assumed to be causing packet contention. Because of this assumption, all traffic from Input Fiber 2 is wavelength converted to the four additional wavelengths available on the Fiber 1 output lines. The four additional wavelengths are connected to Destination 1_5 through Destination 1_8. The switch architecture and the traffic flow for the Single Input Processor Architecture with Four

Wavelength Conversion is shown in Figure 29 on the next page. The traffic flow is represented by the arrows.

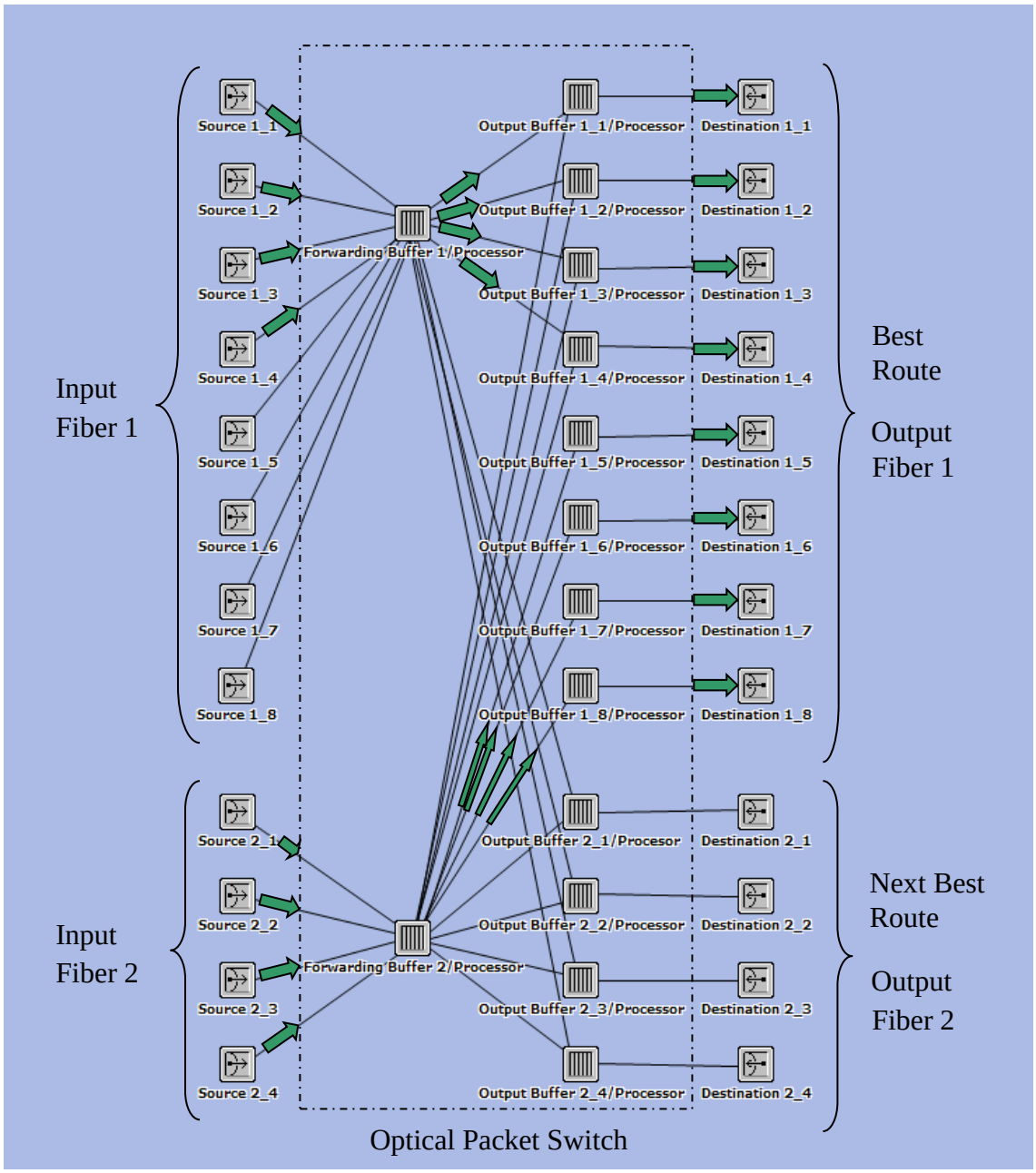

Figure 29 Switch Architecture and Traffic Flow for Single Input Processor with Four Wavelength Conversion

5.5 Single Input Processor Architecture with Three Wavelength Conversion

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. The Single Input Processor Architecture with Three Wavelength Conversion has one forwarding buffer and one output buffer per fiber. Each forwarding buffer has one processor that forwards packets at 10 gigabits per second. Each output buffer also has one processor that forwards packets at 10 gigabits per second. Each fiber has four wavelengths. The traffic on input Fiber 2 is assumed to be causing packet contention. Because of this assumption, all traffic from Fiber 2 is wavelength converted to the three additional wavelengths available on the Fiber 1 output lines. The three additional wavelengths are connected to Destination 1_5 through Destination 1_7. The switch architecture for the Single Input Processor Architecture with Three Wavelength Conversion and the traffic flow for Input Fiber 1 and the First, Second, and Third Source of Input Fiber 2 is shown in Figure 30 on the next page. The traffic flow is represented by the arrows.

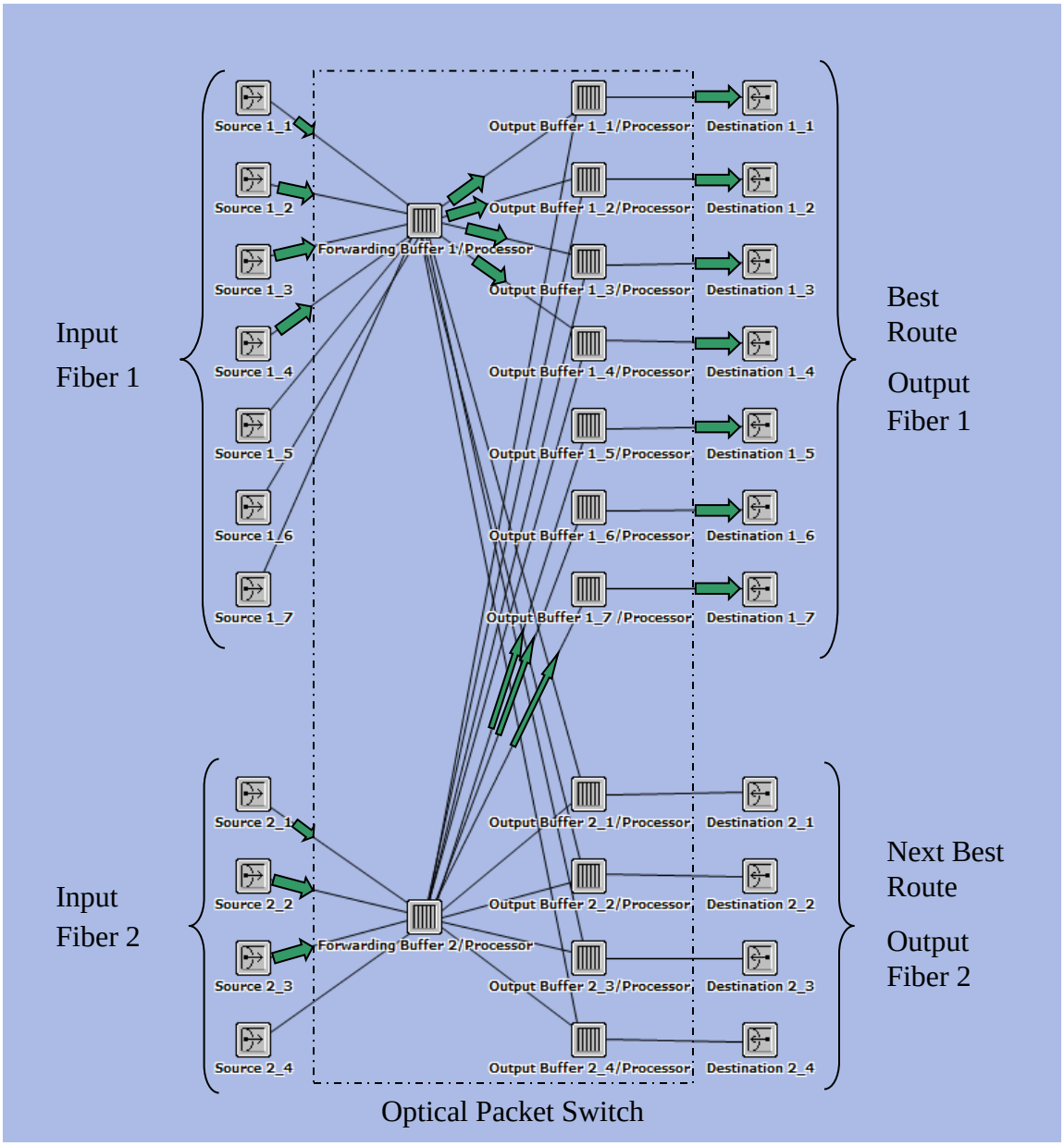

Figure 30 Switch Architecture for Single Input Processor Architecture with Three Wavelength Conversion and the Traffic Flow for Fiber 1 and the First, Second, and Third Source of Fiber 2

The switch architecture for the Single Input Processor Architecture with Three Wavelength Conversion and the traffic flow for the Fourth Source of Input Fiber 2 are shown in Figure 31 on the next page. The traffic flow is represented by the arrows.

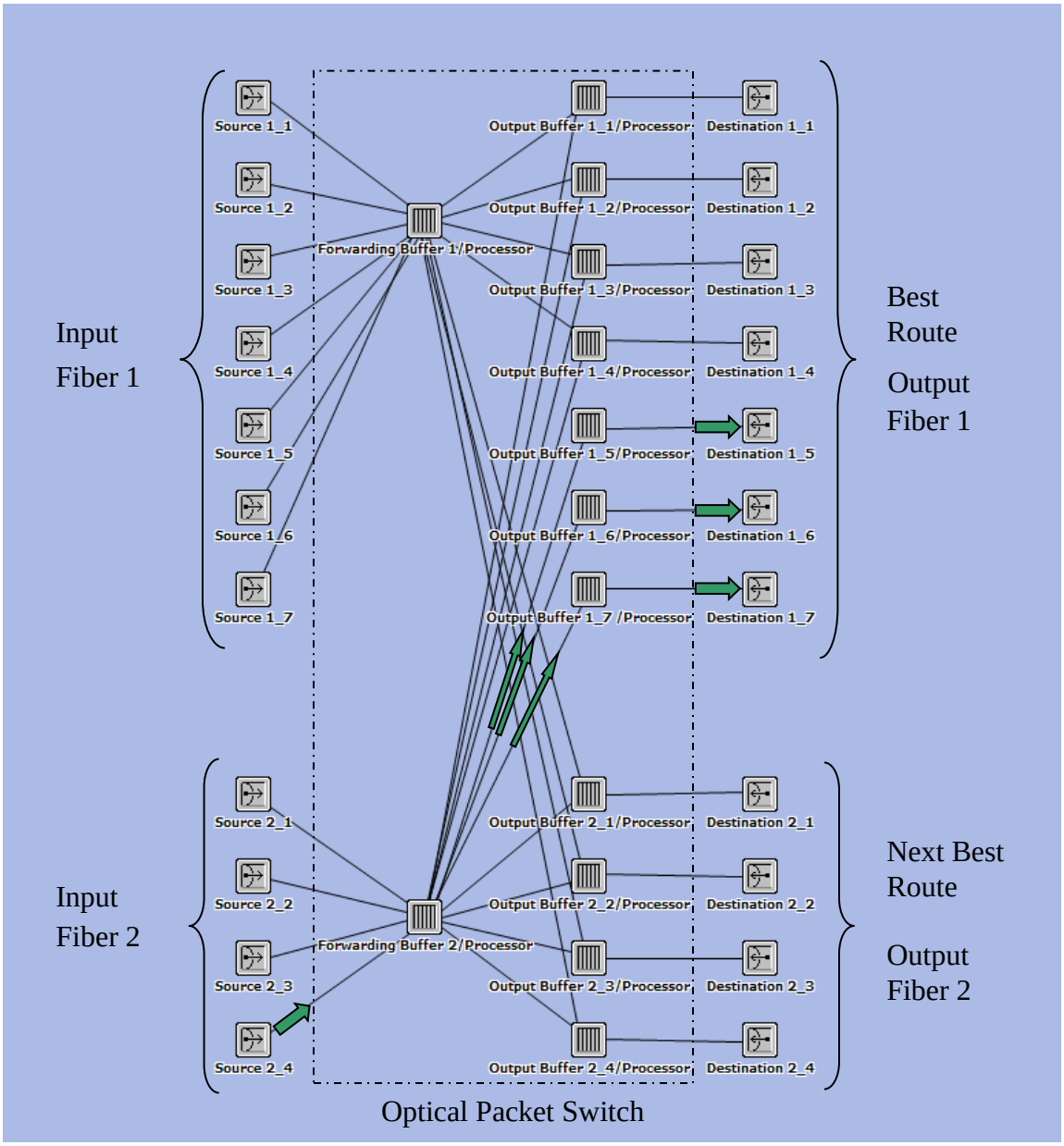

Figure 31 Switch Architecture for Single Input Processor with Three Wavelength Conversion and the Traffic Flow for the Fourth Source of Input Fiber 2

5.6 Single Input Processor Architecture with Two Wavelength Conversion

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. The Single Input Processor Architecture with WC2 has one forwarding buffer and one output buffer per fiber. Each forwarding buffer has one processor that forwards packets at 10 gigabits per second. Each output buffer also has one processor that forwards packets at 10 gigabits per second. Each fiber has four wavelengths. The traffic on Input Fiber 2 is assumed to be causing packet contention. Because of this assumption, all traffic from Input Fiber 2 is wavelength converted to the two additional wavelengths available on the Fiber 1 output lines. The two additional wavelengths are connected to Destination 1_5 and Destination 1_6. The switch architecture for Single Input Processor Architecture with Two Wavelength Conversion and the Traffic Flow for Input Fiber 1 and the First and Second Source of Input Fiber 2 is shown in Figure 32 on the next page. The traffic flow is represented by the arrows.

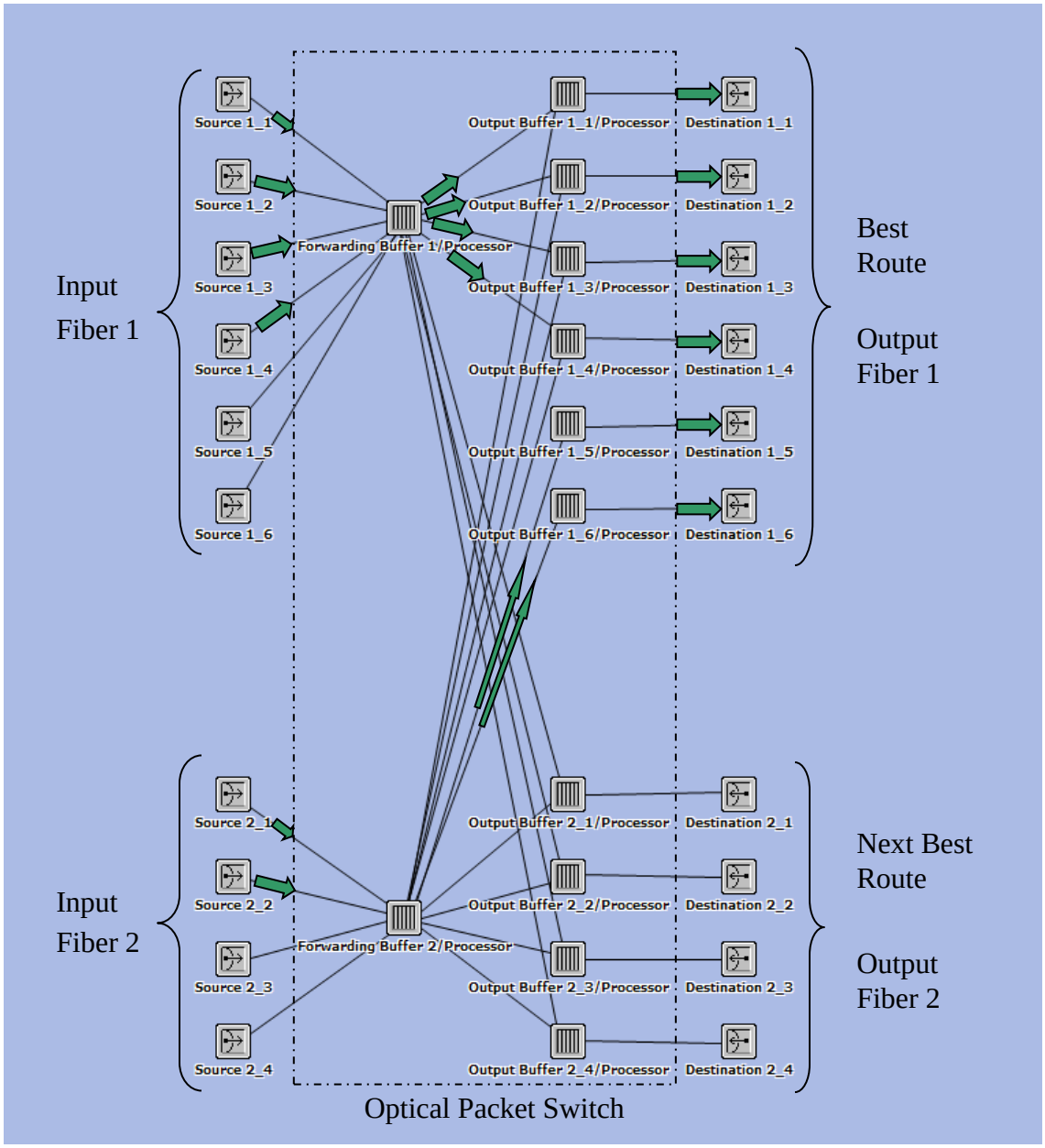

Figure 32 Switch Architecture for Single Input Processor Architecture with Two Wavelength Conversion and the Traffic Flow for Input Fiber 1 and the First and Second Source of Input Fiber 2

The switch architecture for Single Input Processor Architecture with Two Wavelength Conversion and the Traffic Flow for the Third and Fourth Source of Input Fiber 2 is shown in Figure 33 on the next page. The traffic flow is represented by the arrows.

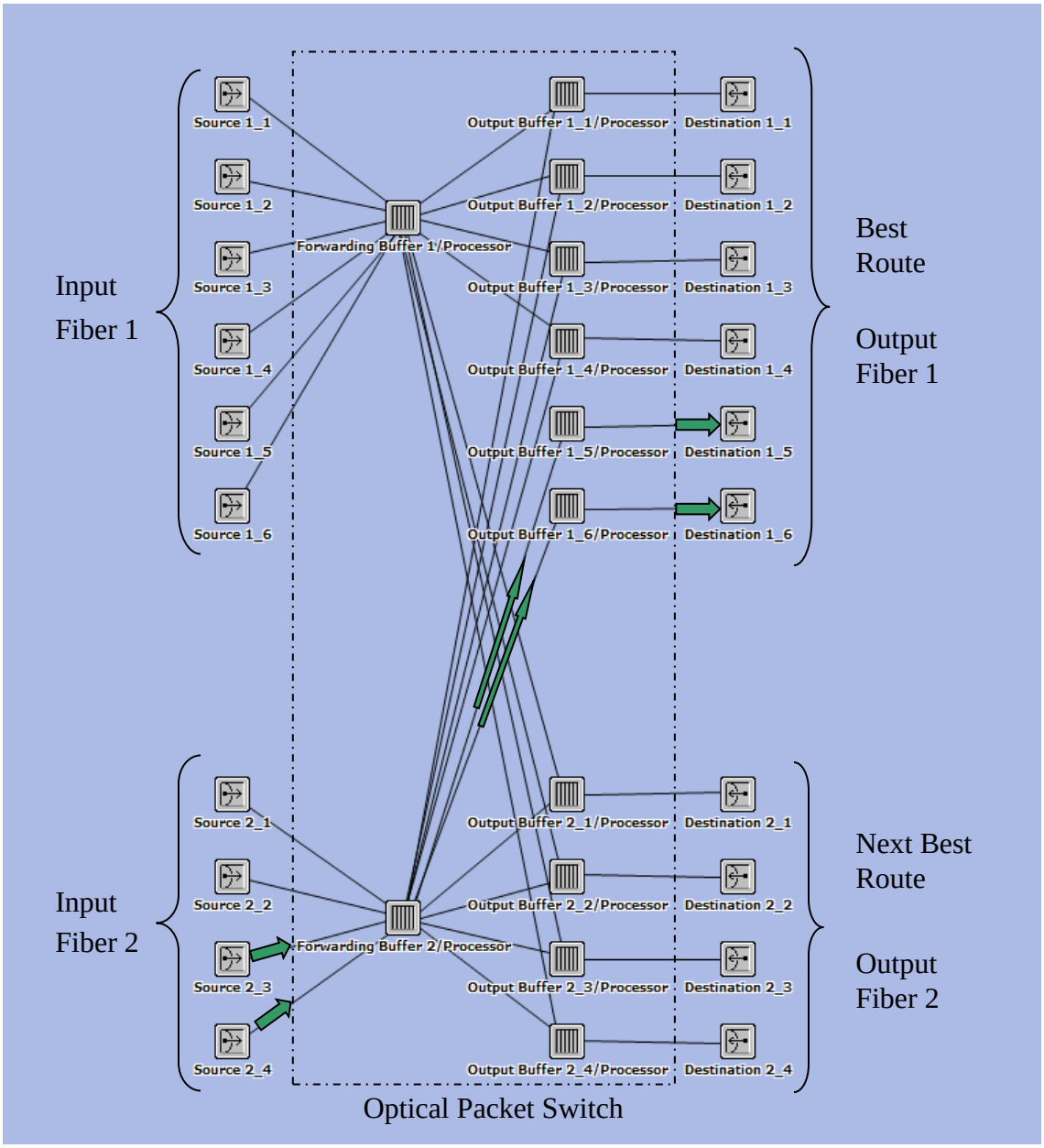

Figure 33 Switch Architecture for Single Input Processor Architecture with Two Wavelength Conversion and the Traffic Flow for the Third and Fourth Source of Input Fiber 2

5.7 Single Input Processor Architecture with One Wavelength Conversion

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. The Single Processor with One Wavelength Conversion scenario has one forwarding buffer and one output buffer per fiber. Each forwarding buffer has one processor that forwards packets at 10 gigabits per second. Each output buffer also has one processor that forwards packets at 10 gigabits per second. Each fiber has four wavelengths. The traffic on Input Fiber 2 is assumed to be causing packet contention. Because of this assumption, all traffic from Fiber 2 is wavelength converted to the additional wavelength available on the Fiber 1 output lines. The additional wavelength is connected to Destination 1_5. The switch architecture and the traffic flow for the Single Input Processor Architecture with One Wavelength Conversion is shown in Figure 34 on the next page. The traffic flow is represented by the arrows.

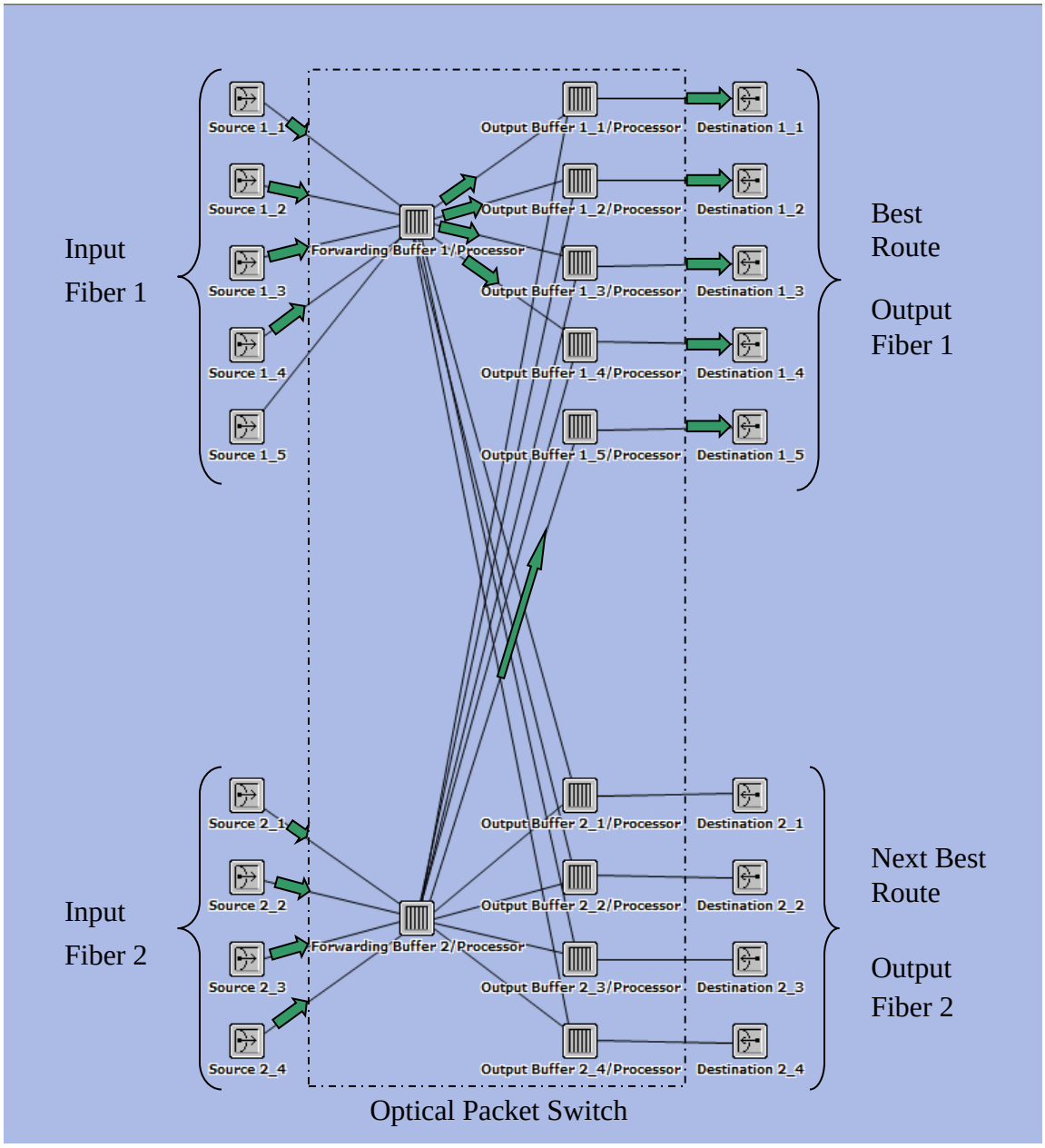

Figure 34 Switch Architecture and Traffic Flow for Single Input Processor Architecture with One Wavelength Conversion

5.8 Parallel Input Processors Architecture

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. All packets generated by the sources are a constant 1500 bytes. All traffic sources forwards packets at 10 gigabits per second. Traffic from Input Fiber 1 is sent to Output Fiber 1 on the same wavelength. This represents the shortest path. Each forwarding buffer and output buffer forwards packets at 10 gigabits per second. Each forwarding buffer has 3200 bytes of storage capacity. Each output buffer has 1600 bytes of storage capacity. Traffic from input Fiber 2 is sent to output Fiber 1. Simulations were run for traffic being generated on each wavelength for 0.1, 2, 4, 6, 8, and 10 gigabits per second. The switch architecture and traffic flows for the Parallel Input Processor Architecture are shown in Figure 35 on the next page.

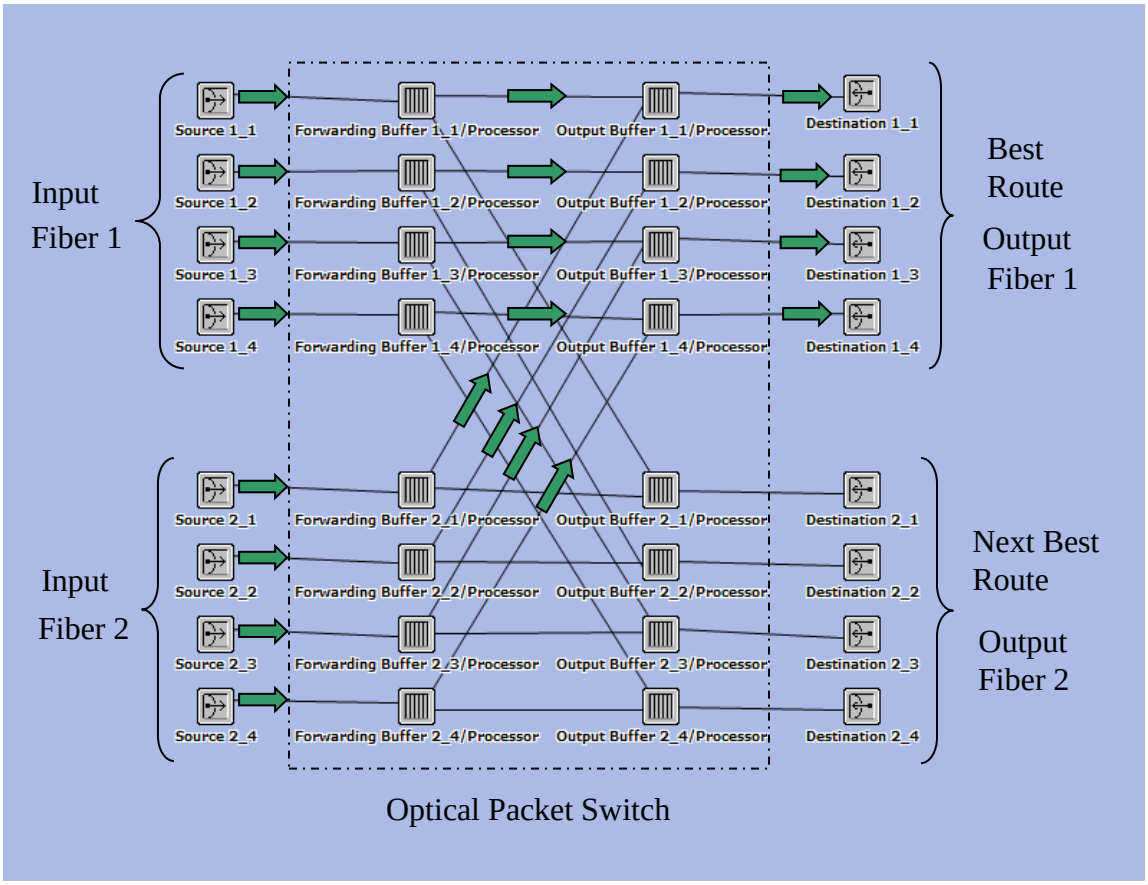

Figure 35 Switch Architecture and Traffic Flow for Parallel Input Processors Architecture

5.9 Parallel Input Processors Architecture with One Wavelength Conversion

There are two fibers connected to the optical packet switch input and two fibers are connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. All packets generated by the sources are a constant 1500 bytes. All traffic sources forwards packets at 10 gigabits per second. Traffic that is generated in Input Fiber 1 is sent to Output Fiber 1 on the same wavelength.

Traffic that is generated from Input Fiber 2 is sent to Destination 1_5 on Output Fiber 1. Each forwarding buffer and each output buffer forward traffic at 10 gigabits per second. Each forwarding buffer has 3200 bytes of storage capacity. Each output buffer has 1600 bytes of storage capacity. The traffic flow represented by arrows and the switch architecture is shown Figure 36 on the next page. Simulations were run for traffic being generated on each wavelength for 0.1, 2, 4, 6, 8, and 10 gigabits per second.

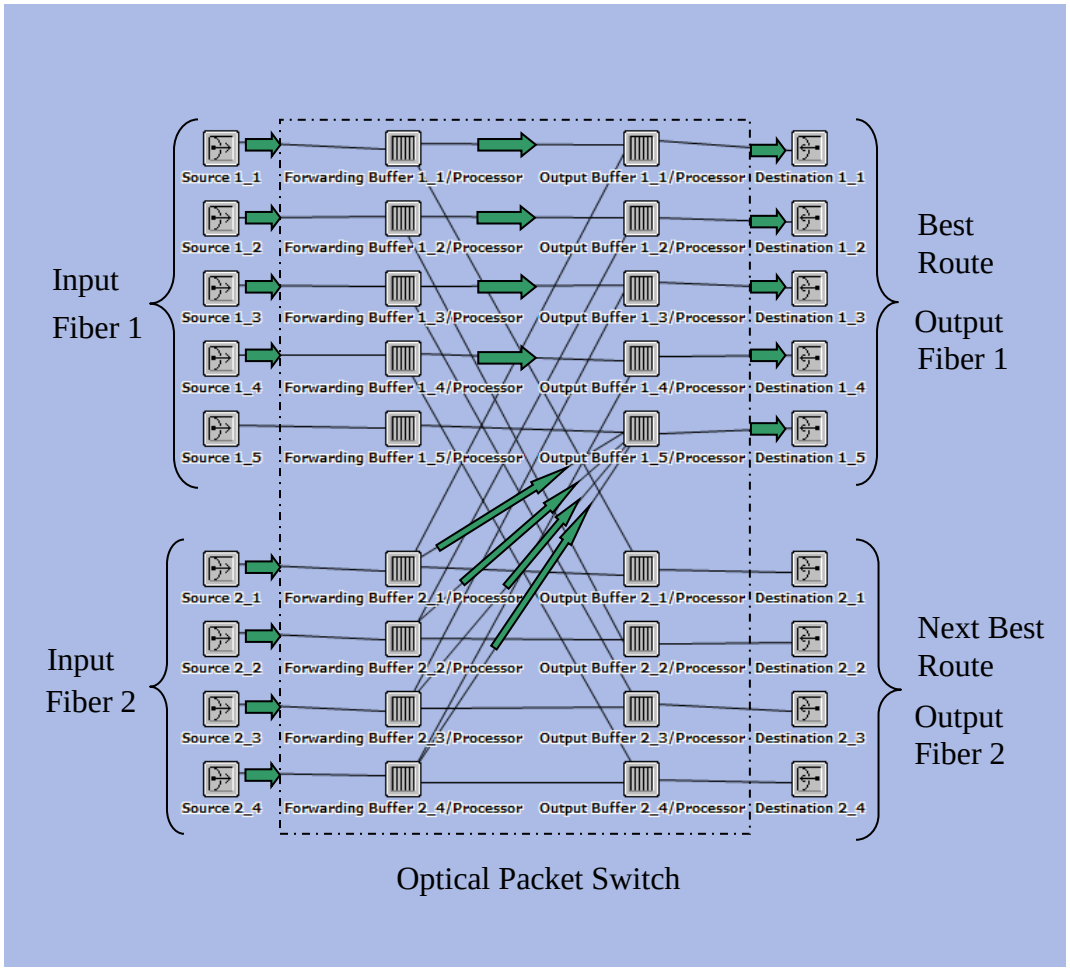

Figure 36 Switch Architecture and Traffic Flow for Parallel Input Processors One Wavelength Conversion

5.10 Parallel Input Processors Architecture with Two Wavelength Conversion

There are two fibers connected to the optical packet switch fiber input connections and two fibers are connected to the switch output fiber connections. Each input fiber has four sources generating traffic. There is one source per wavelength. All packets generated by the sources are a constant 1500 bytes. All traffic sources forwards packets at 10 gigabits per second. Traffic that is generated in input Fiber 1 is sent to output Fiber 1 on the same wavelength. Traffic that is generated from input Fiber 2 is sent to Destination 1_5 and Destination 1_6 on Output Fiber 1. The traffic flow is represented by arrows, and the network architecture is shown in Figure 37 on the next page and on the page after in Figure 38. Each forwarding buffer and each output buffer forward traffic at 10 gigabits per second. Each forwarding buffer has 3200 bytes of storage capacity. Each output buffer has 1600 bytes of storage capacity. Simulations were run for traffic being generated on each wavelength for 0.1, 2, 4, 6, 8, and 10 gigabits per second.

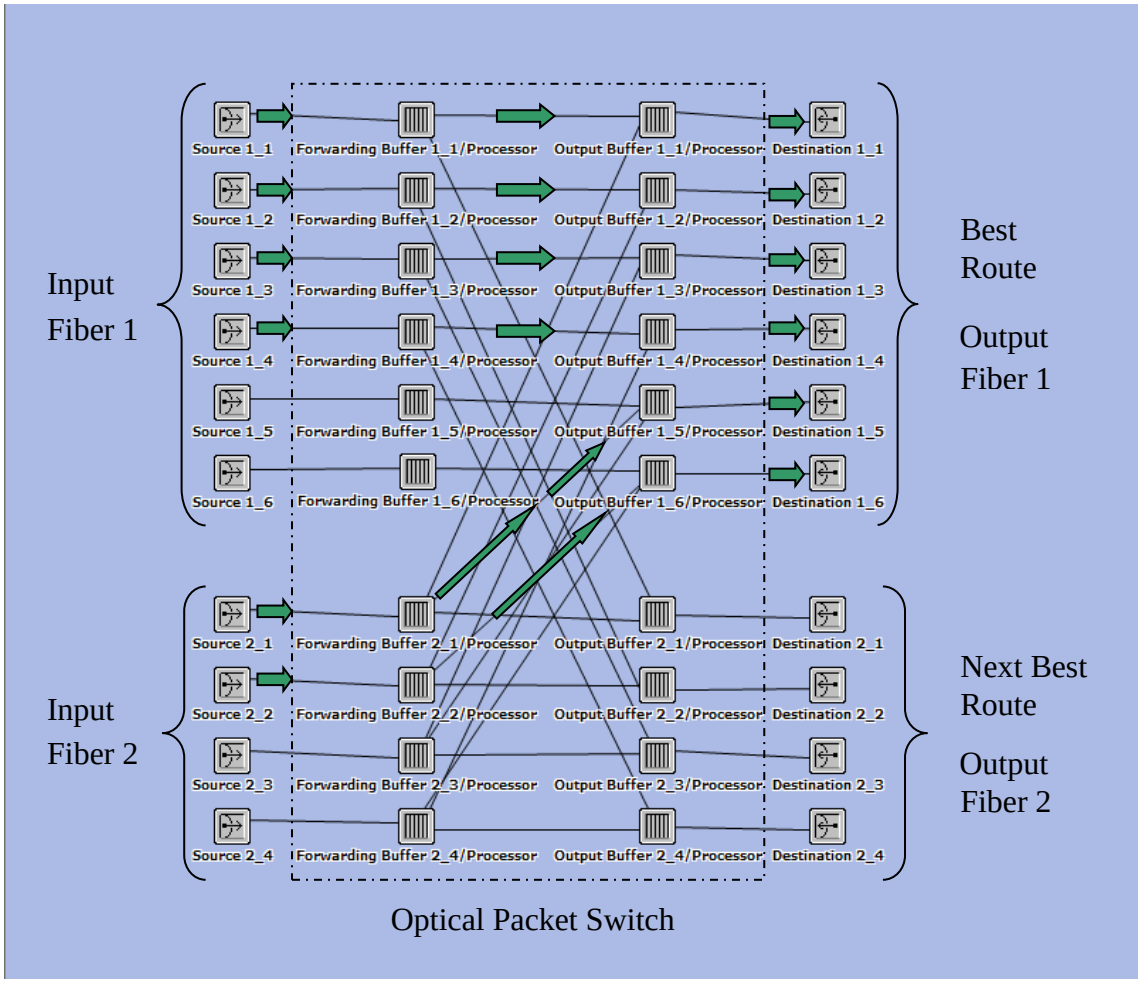

Figure 37 Switch Architecture for Parallel Input Processors Architecture with Two Wavelength Conversion and the Traffic Flow for Fiber 1 and the First and Second Source of Fiber 2

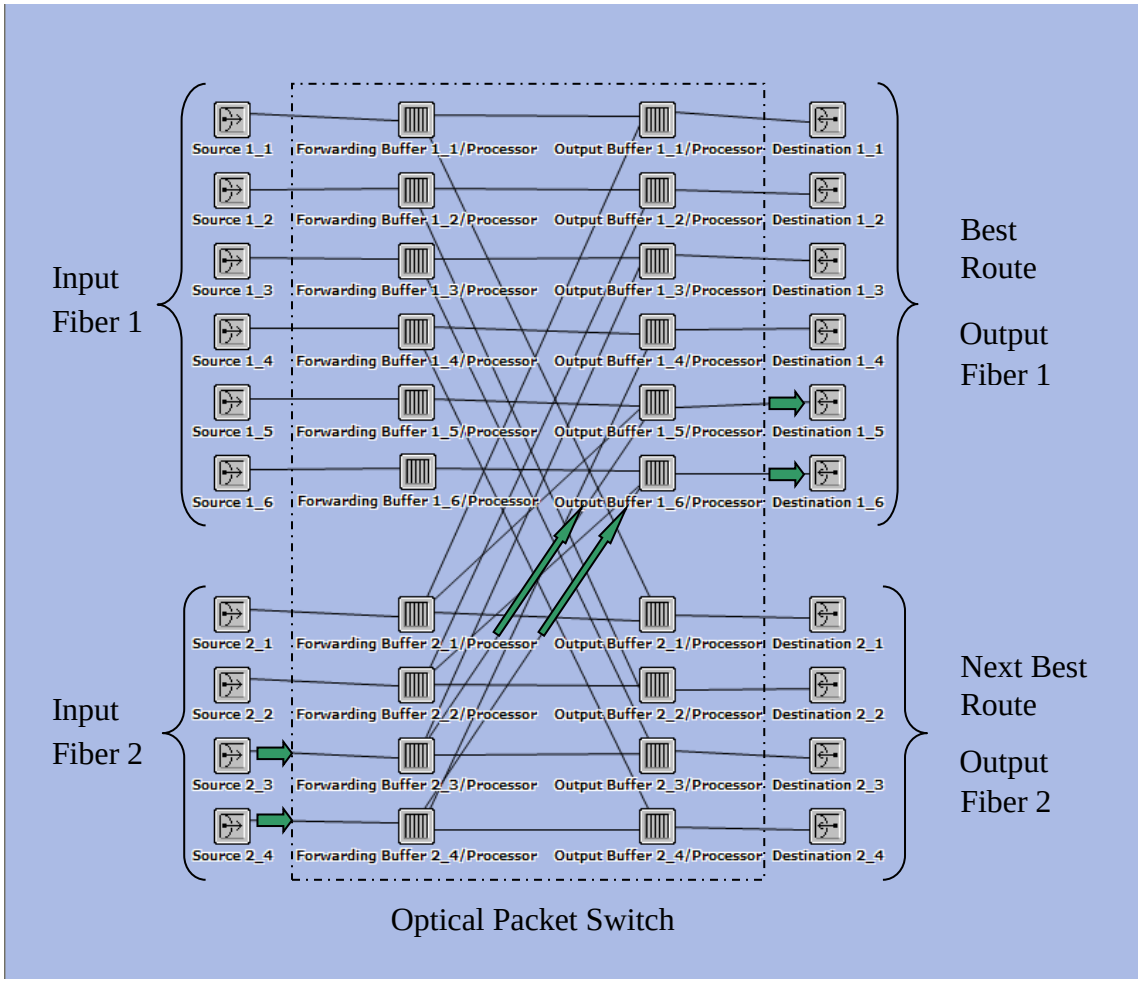

Figure 38 Switch Architecture for Parallel Input Processors Architecture with Two Wavelength Conversion and the Traffic Flow for the Third and Fourth Source of Fiber 2

5.11 Parallel Input Processors Architecture with Three Wavelength Conversion

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each fiber has four sources generating traffic. There is one source per wavelength. All packets generated by the sources are a constant 1500 bytes. All traffic sources forwards packets at 10 gigabits per second. Traffic that is generated in Input Fiber 1 is sent to Output Fiber 1. All traffic from Input Fiber 1 stays on the same wavelength when transferred to Output Fiber 2. Traffic that is generated from Input Fiber 2 is sent to Destination 1_5 through Destination 1_7 of Output Fiber 1. This traffic represents the wavelength converted traffic. The traffic from Source 2_1 is routed through Forwarding Buffer 2_1 through Output Buffer 1_5. The traffic from Source 2_2 is routed through Forwarding Buffer 2_2 through Output Buffer 1_6. The traffic from Source 2_3 is routed through Forwarding Buffer 2_3 through Output Buffer 1_7. The traffic flow and the switch architecture are shown with arrows in Figure 39. The traffic from Source 2_4 is routed through Forwarding Buffer 2_4 and equally distributed through Output Buffer 1_5, Output Buffer 1_6, and Output Buffer 1_7. The first packet generated by Source 2_4 is sent to Output Buffer 1_5 through Forwarding Buffer 2_4. The second packet generated by Source 2_4 is sent to Output Buffer 1_6 through Forwarding Buffer 2_4. The third packet generated by Source 2_4 is sent to Output Buffer 1_7 through Forwarding Buffer 2_4. The routing process for Source 2_4 repeats itself to the end of the simulation. The traffic flow and the switch architecture are shown with arrows representing the traffic flow in

Figure 40. Each forwarding buffer and each output buffer forward traffic at 10 gigabits per second. Each forwarding buffer has 3200 bytes of storage capacity. Each output buffer has 1600 bytes of storage capacity. Simulations were run for traffic being generated on each wavelength for 0.1, 2, 4, 6, 8, and 10 gigabits per second.

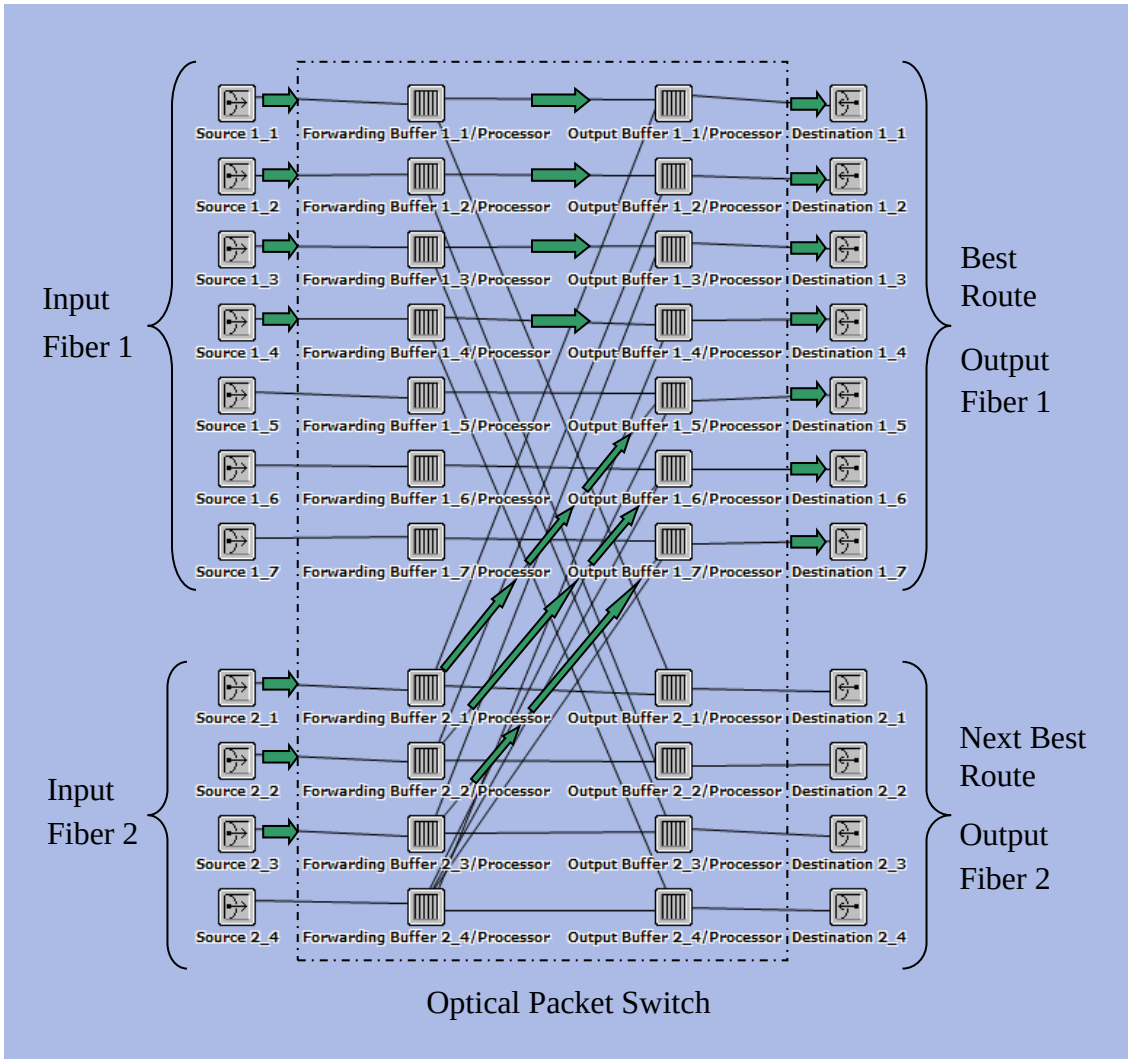

Figure 39 Switch Architecture for Parallel Input Processors Architecture with Three Wavelength Conversion and the Traffic Flow for Fiber 1 and the First, Second and Third Source of Fiber 2

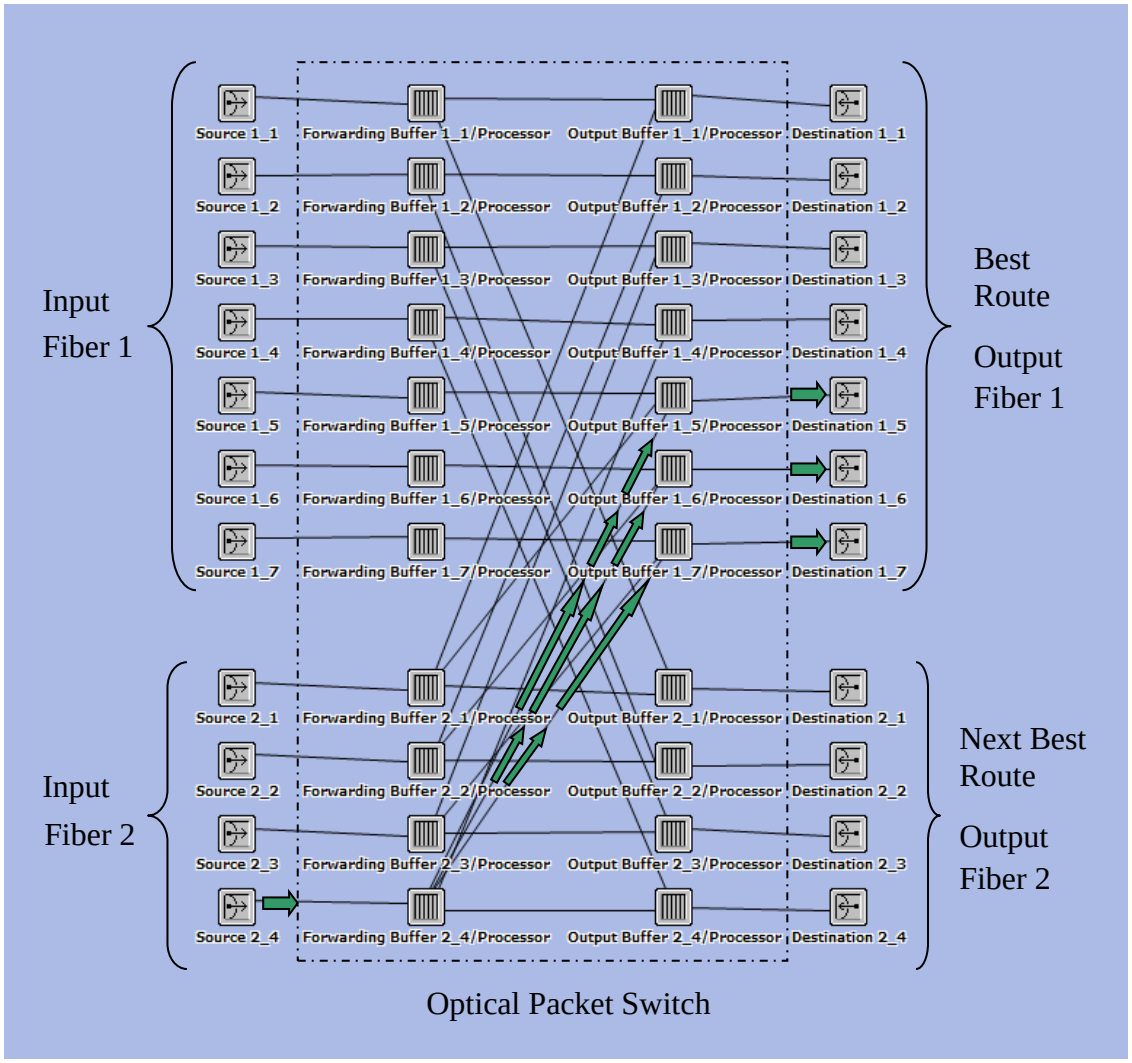

Figure 40 Switch Architecture for Parallel Input Processors Architecture with Three Wavelength Conversion and the Traffic Flow for the Fourth Source of Fiber 2

5.12 Parallel Input Processors Architecture with Next Best Route

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each fiber has four sources generating traffic. There is one source per wavelength. All packets generated by the sources are a constant 1500 bytes. All traffic sources forwards packets at 10 gigabits per second. All traffic generated on Input Fiber 1 is sent to Output Fiber 1. This represents the shortest path. All traffic transferred from Input Fiber 1 to Output Fiber 1 is transferred on the same wavelength. All traffic generated on Input Fiber 2 is normally sent to Output Fiber 1 but is sent to Output Fiber 2 on the same wavelength. This route represents the Next Best Route. In this switch architecture and routing protocol, traffic is distributed over eight output lines. All of the previously described scenarios have traffic distributed over four output lines. Traffic is forwarded at 10 gigabits per second at each forwarding buffer and at each output buffer. Simulations were run for traffic being generated on each wavelength for 0.1, 2, 4, 6, 8, and 10 gigabits per second. The switch architecture and traffic flows represented by arrows are shown in Figure 41 on the next page for the Parallel Input Processor Architecture with Next Best Route.

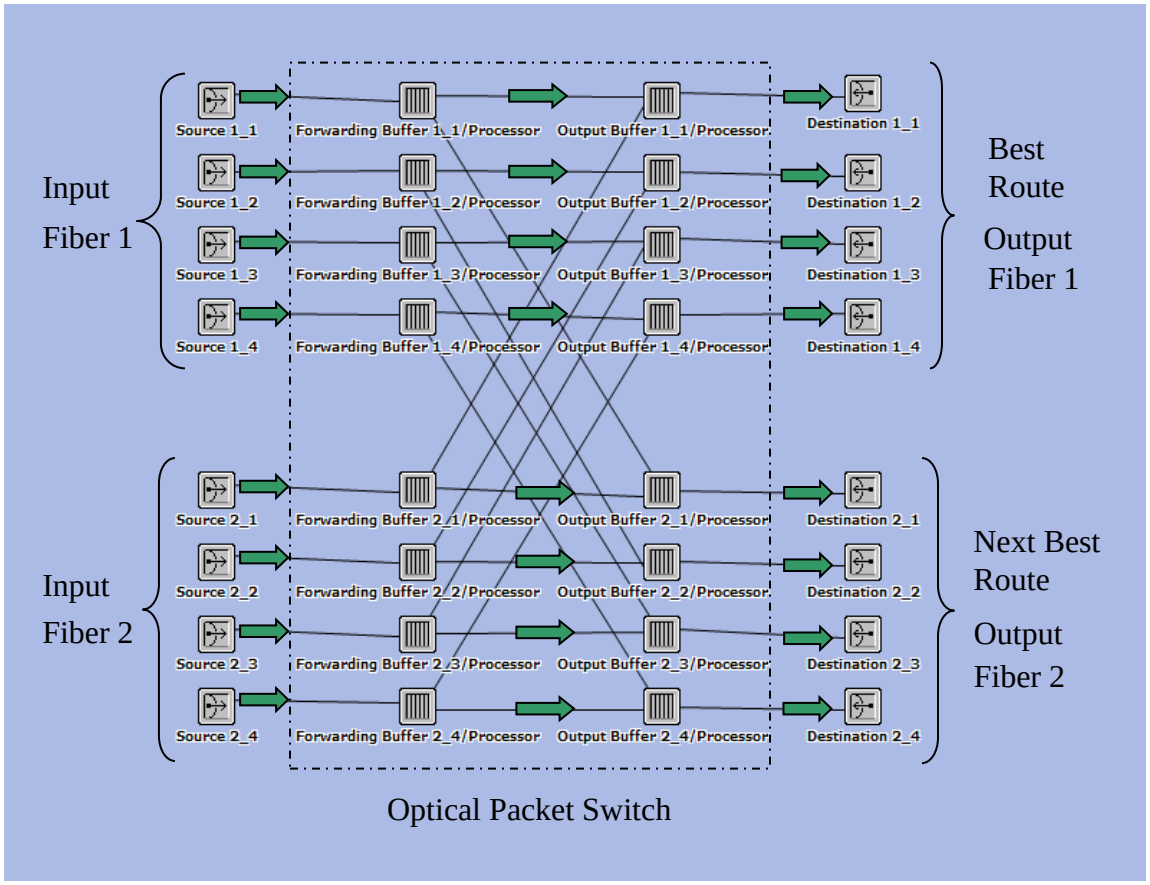

Figure 41 Switch Architecture and Traffic Flow for Parallel Input Processors Architecture with Next Best Route

5.13 Parallel Input Processors Architecture with Four Wavelength Conversion

There are two fibers connected to the optical packet switch fiber input connections and two fibers connected to the switch output fiber connections. Each fiber has four sources generating traffic. There is one source per wavelength. All packets generated by the sources are a constant 1500 bytes. All traffic sources forwards packets at 10 gigabits per second. All traffic generated in Input Fiber 1 is sent to Output Fiber 2. Traffic from Input Fiber 1 that is transferred to Output Fiber 2 will be transferred on the same wavelength. Traffic that is generated Input Fiber 2 is sent to Destination 1_5 through Destination 1_8 on Output Fiber 1. This traffic represents the wavelength converted traffic. Each forwarding buffer and each output buffer forward traffic at 10 gigabits per second. Each forwarding buffer has 3200 bytes of storage capacity. Each output buffer has 1600 bytes of storage capacity. Simulations were run for traffic being generated on each wavelength for 0.1, 2, 4, 6, 8, and 10 gigabits per second. The switch architecture and traffic flows are shown on the next page in Figure 42 for the Parallel Input Processor Architecture with Four Wavelength Conversion. The traffic flows are represented by the arrows.

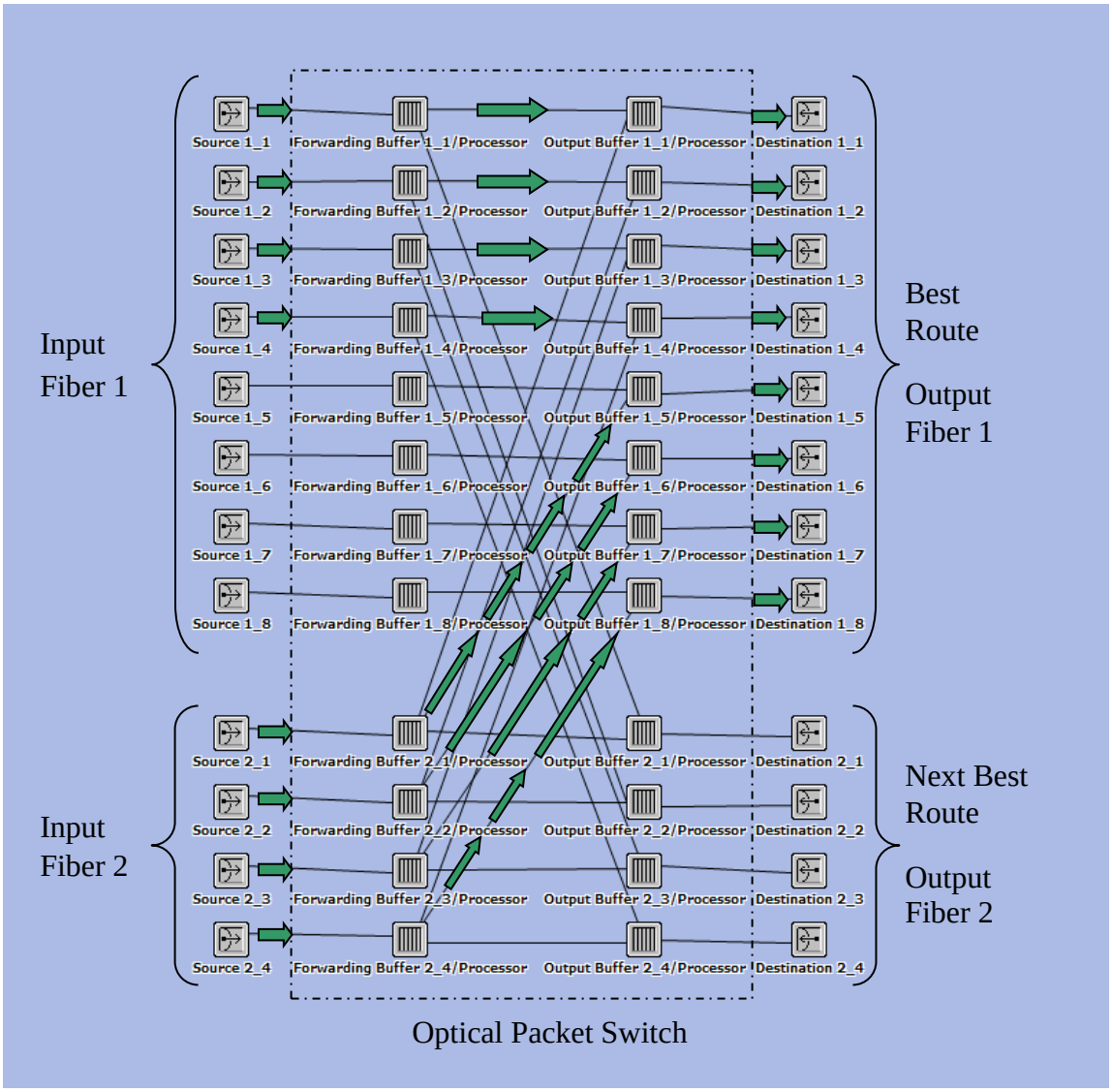

Figure 42 Switch Architecture and Traffic Flow for Parallel Input Processors Architecture with Four Wavelength Conversion

5.14 Description of OPNET Simulation

All simulations were performed using OPNET Modeler. The sources, buffers, links, and destinations were constructed using OPNET Modeler's standard models. Traffic was generated using the ppp_ip_station model. All links were constructed using the ppp_adv link model. All forwarding buffers were constructed using slip16_gtwy_adv router model. All output buffers were constructed using the slip16_gtwy_adv router model. All destination models were constructed using the ppp_server model.

The following data was collected from OPNET Model on each simulation run. The number packets sent by each source on every input channel of the switch. The number of packets received on each channel the number of packets sent by each channel, and the number of packets dropped for each channel at the forwarding buffer and the output line buffer. The average throughput on each output channel of the switch.

Chapter 6 Results

6.1 Metrics

The metrics that were calculated for the results were packet loss rate, average throughput per line, and total throughput. The packet-loss rate is the total number of dropped packets divided by the total number of packets received at the switch. The average throughput per line is the average of each line throughput. The throughput of each line is the average number of bits successfully transmitted by each output buffer per unit time, in bits per second. The total throughput is the sum of each line average throughput.

6.2 List of Architectures

The following architectures were modeled, simulated and evaluated using OPNET Modeler.

The simplest architectures were evaluated first. The Baseline architecture had the simplest architecture and no packet contention resolution. The Single Input Processor architecture with one output line processor per line was evaluated next. Then the Single Input Processor architecture with packet contention resolution was evaluated next. Evaluation of the results determined the Single Input Processor architecture would not provide the desired results. The Parallel Input Processor architecture was evaluated next without any packet contention resolution. The Parallel Input Processor architecture with packet contention resolution was evaluated next.

1. Baseline (Single Input & Output Processor, no wavelength conversion, no Next Best Route)
2. Single Input Processor (no contention resolution)
3. Single Input Processor with Next Best Route
4. Single Input Processor with 4 Wavelength Conversion
5. Single Input Processor with 3 Wavelength Conversion
6. Single Input Processor with 2 Wavelength Conversion
7. Single Input Processor with 1 Wavelength Conversion
8. Parallel Input Processor
9. Parallel Input Processor with 1 Wavelength Conversion
10. Parallel Input Processor with 2 Wavelength Conversion
11. Parallel Input Processor with 3 Wavelength Conversion
12. Parallel Input Processor with 4 Wavelength Conversion
13. Parallel Input Processor with Next Best Route

The processor speed for the architectures listed is 10 gigabit/sec. The architectures listed have two input fibers and four lines per fiber. The architectures listed without wavelength conversion have two output fibers and four output lines. The architectures listed with wavelength conversion have two output fibers and four output lines and the number of wavelength conversion lines specified in the architecture name. The Parallel Input Processor architecture has one processor per line in the forwarding buffer.

6.3 List of Group of Architectures

The following groups of architectures were modeled and simulated.

1. Baseline – (Single input and output processors, no wavelength conversion or Next Best Route)
2. Single Input Processor with Wavelength Conversion
3. Single & Parallel Input Processor with/wo Next Best Routes
4. Parallel Input Processor with Wavelength Conversion
5. Parallel Input Processor with Four Wavelength Conversion
6. Single & Parallel Input Processor with Four Wavelength Conversion

A Baseline group was established so that performance could be evaluated for architectures without contention resolution techniques. The Single Input Processor with Wavelength Conversion group was created to study the effects wavelength conversion with Single Input Processor architecture. The Single and Parallel Input Processor with and without Next Best Routes was created to study how Next Best Route affects packet contention resolution on both Single Input Processor architecture and the Parallel Input Processor architecture. The Parallel Input Processor with Wavelength Conversion group was created to study the effect of wavelength conversion on the Parallel Input Processor architecture. The Parallel Input

Processor with Four Wavelength Conversion group was created to study the effect of data rates greater than 10 gigabits per second on performance. The Single and Parallel Input Processor with Four Wavelength Conversion group was created to study the effect of input processor architecture on performance.

The dissertation is trying to show that packet contention can be reduced and eliminated in an optical packet switch using 10 gigabit per second processors in an optical network with 10 gigabit per second line rates. The packet contention resolution techniques incorporate wavelength conversion and Next Best Route routing into the packet contention resolution techniques. There is a need to reduce packet conflict. Previous studies show packet loss rates greater than 0.01.

All architectures except the baseline architecture have multiple (one per wavelength) output processors. Each processor has a processing speed of 10 Gbps.

6.4 Packet Loss Rate for Single and Parallel Input Processors Architectures

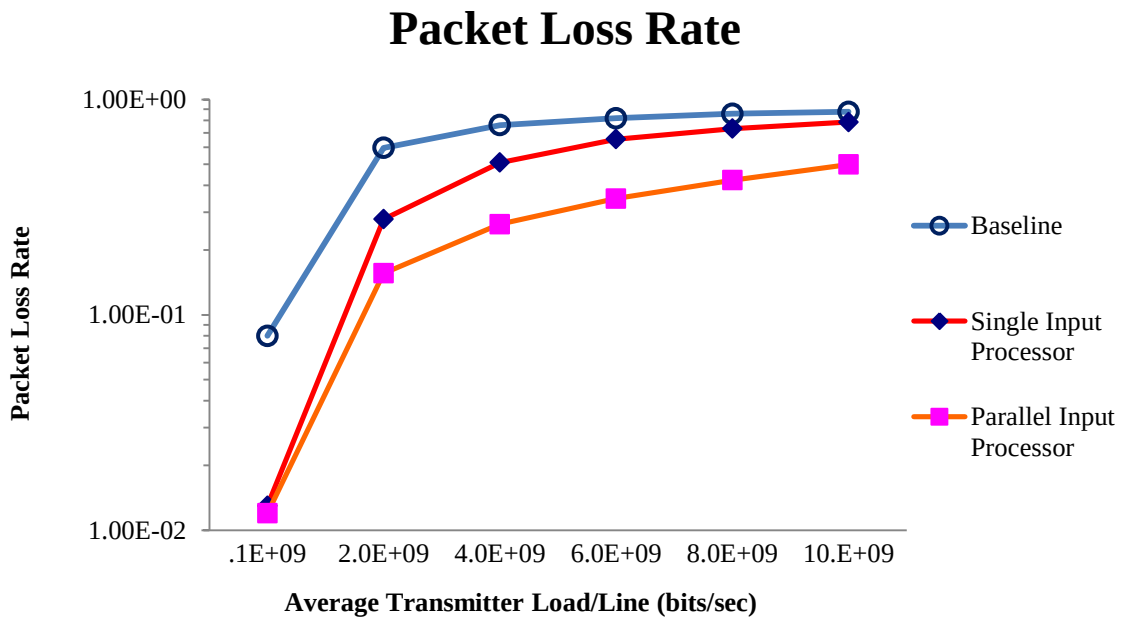

Figure 43 Packet Loss Rate for Baseline, Single and Parallel Input Processors Architectures

The packet loss rate for the Baseline architecture, Single Input Processor architecture, and Parallel Input Processors architecture is shown above in Figure 43. The packet loss rate is the highest for the Baseline architecture due to high packet loss at the forwarding buffer and the output buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow the forwarding buffer. The packet loss rate is lower for the Single Input Processor architecture than the Baseline architecture. The packet loss rate is lower because the packet loss at the output optical buffer is lower. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce

packet loss. The first improvement to the output buffer architecture is to have one output buffer per wavelength. The second improvement is to have one processor per wavelength to forward packets to the next switch or network device. This improvement resulted in having two additional buffers to delay packets at each output fiber. The packet loss rate is even lower for the Parallel Input Processor architecture. The packet loss rate is the lowest of the three architectures because packet loss is reduced at both the forwarding buffers and the output buffers. The Parallel Input Processor architecture has two inprovements to its forwarding buffer archtecture to reduce packet loss. The architecure improvements to the forward buffer is to have one forwarding processor per wavelength and one forwarding buffer per wavelength that can delay two packets. The Parallel Input Processor also has the architecure improvement to epimprovement to reduce packet loss. For all the architectures the packet loss is unacceptable, so the regular, single and parallel input processors architecture is not viable. Additional packet conflict resolution techniques are needed.

6.5 Average Throughput Per Line for Single and Parallel Input Processors Architectures

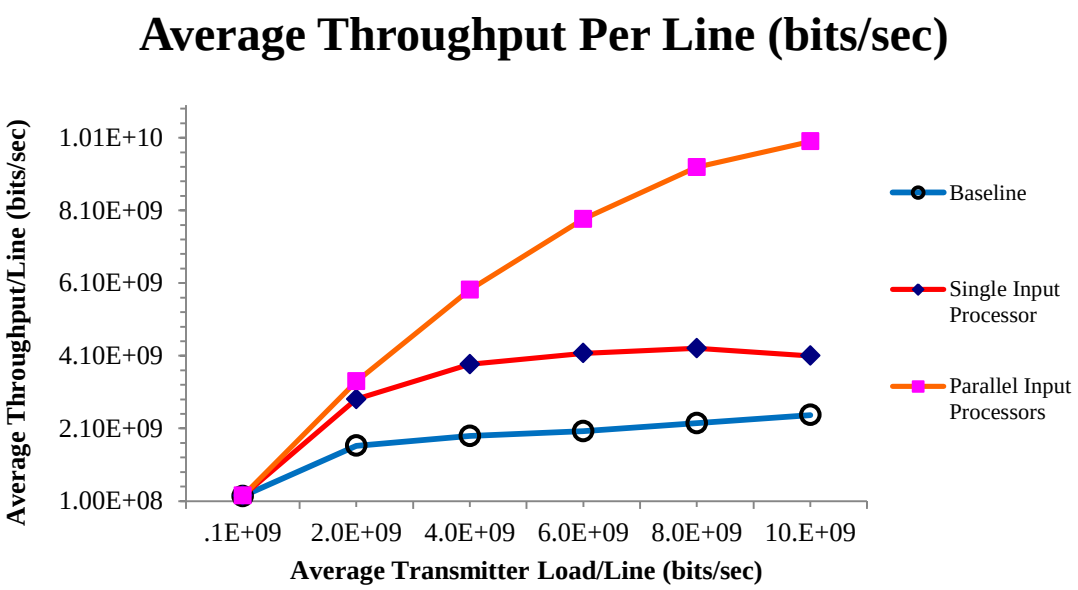

Figure 44 Average Throughput per Line for Baseline, Single and Parallel Input Processors Architectures

The average throughput per line for the Baseline architecture, Single Input Processor architecture, and the Parallel Input Processors architecture is shown above in Figure 44. The Baseline architecture has the lowest Average Throughput per line. The average throughput per line is the lowest for the Baseline architecture because of high packet loss at both the forwarding buffer and the output buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow the forwarding buffer. The Single Input Processor architecture has higher average throughput per line than the Baseline architecture. This is due to reduced packet loss at the output buffer. The Single

Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one buffer per wavelength resulting in an increase of two additional buffers to delay packets per output fiber. The Parallel Input Processors architecture has the highest average throughput per line. The Parallel Input Processors has improvements to its forwarding buffer architecture and its output buffer to reduce packet loss and to increase the average throughput per line. Packet loss was reduced in the forwarding processors by having one forwarding processor per wavelength to forward packets to the output buffers and by having one forwarding buffer per wavelength to delay packets. The eight forwarding processors were able to forward all the incoming packets from the eight input lines into the four output lines on output Fiber 1. The output buffer of the Parallel Input Processor architecture has the same architecture improvement as the Single Input Processor output buffer. For all the architectures the packet loss is unacceptable, so the regular, single and parallel input processors architecture is not viable. Additional packet conflict resolution techniques are needed.

6.6 Total Throughput for Single and Parallel Input Processors Architectures

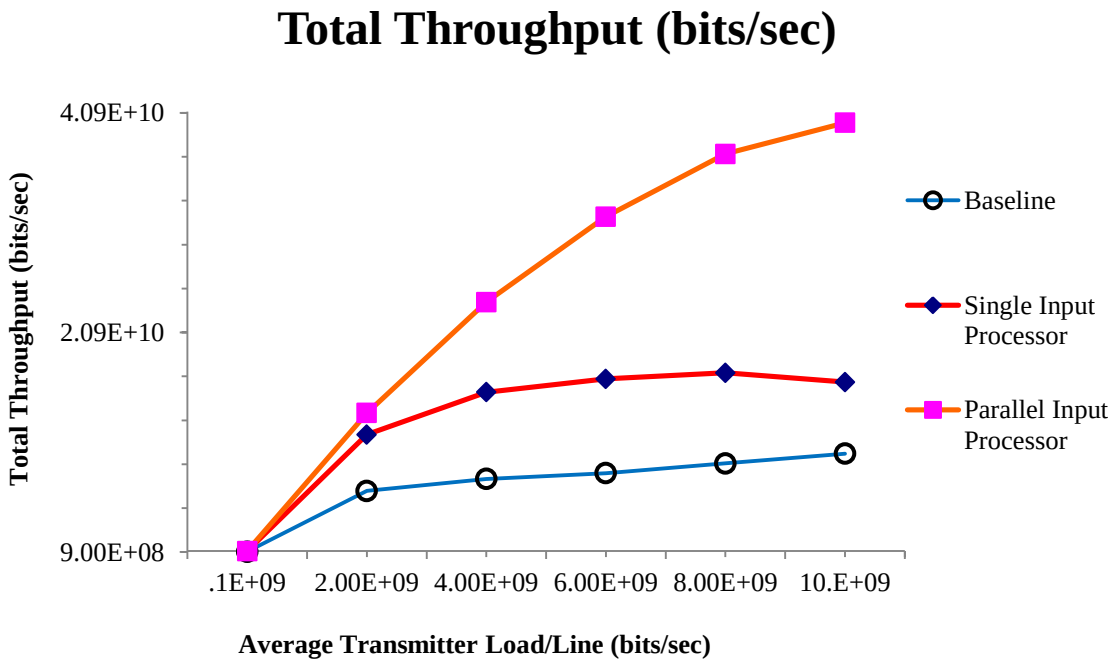

Figure 45 Total Throughput for Baseline, Single and Parallel Input Processors Architectures

The total throughput for the Baseline architecture, the Single Input Processor architecture, and the Parallel Input Processors architecture is shown above in Figure 45. The Baseline architecture has the lowest total throughput. The total throughput is the lowest for the Baseline architecture because of high packet loss at the forwarding buffer and the output buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow the forwarding buffer. The Single Input Processor architecture has higher total throughput than the Baseline architecture due to

reduced packet loss at the output buffers. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss and increase the total throughput. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one buffer per wavelength resulting in an increase of two additional buffers to delay packets at each output fiber. The Parallel Input Processors architecture has the highest total throughput. The higher total throughput is attributed reduced packet loss at the forwarding buffer and the output buffer. Packet loss at the forwarding buffer is reduced by having one forwarding processor per wavelength to forward packets to the output buffer and by having one forwarding buffer per wavelength to delay the incoming packets. The eight processors at the forwarding buffers were able to forward all incoming packets from eight input lines into four output lines. The output buffer of the Parallel Input Processor architecture has the same architecture improvement as the Single Input Processor output buffer. For all the architectures the packet loss is unacceptable, so the regular, single and parallel input processors architecture is not viable. Additional packet conflict resolution techniques are needed.

6.7 Packet Loss Rates for Single Input Processor Architecture with Wavelength Conversion

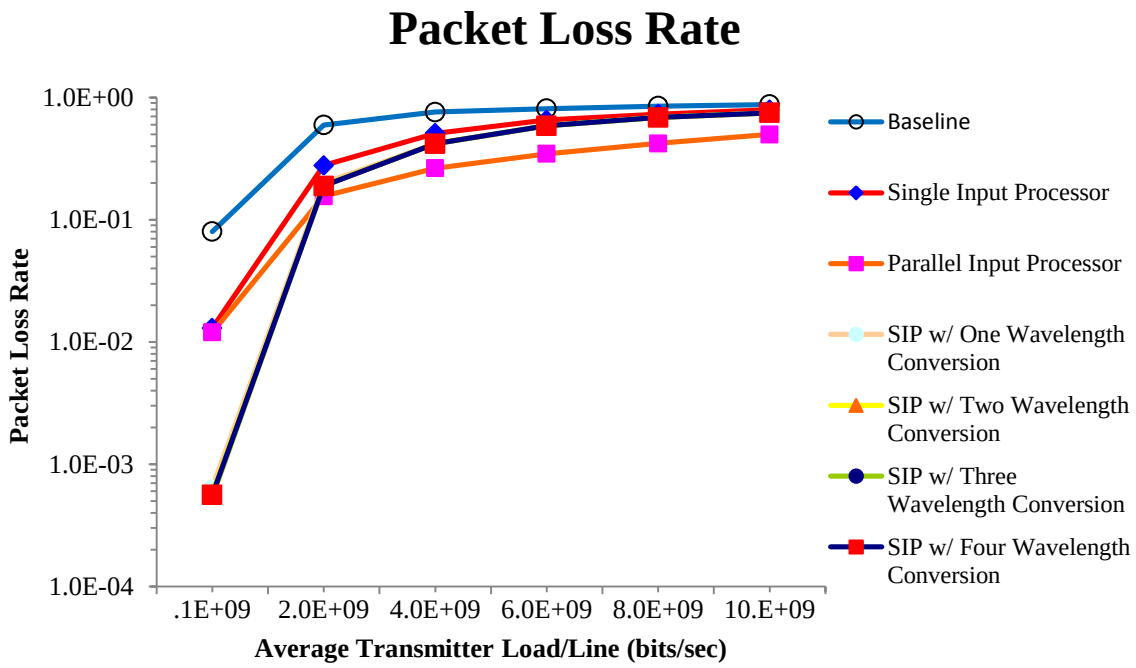

Figure 46 Packet Loss Rates for Baseline, Single Input Processor Architecture with and without Wavelength Conversion, Parallel Input Processors Architecture

The packet loss rate for the Baseline architecture, Single Input Processor architecture, Single Input Processor architecture with one, two, three, and four wavelength conversions is shown above in Figure 46. The packet loss rate is the highest for the Baseline architecture due to high packet loss at the forwarding buffer and the output buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing the forwarding buffer to overflow. The packet loss rate is lower for the Single Input Processor architecture. The packet loss rate is lower because the packet loss at the output optical buffer is lower.

The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one output buffer per wavelength. This resulted in two additional buffers to delay packets per output fiber. The packet loss rate for the Single Input Processor architectures with wavelength conversion showed little improvement over the Single Input Processor architecture for average transmitter load per line of 6.0 gigabits per second. There was limited improvement for the packet loss rate for the Single Input Processors with wavelength conversion over the Single Input Processor architecture from 1.0 gigabits per second to 6.0 gigabits per second. From 0.1 gigabits per second to 1.0 gigabits per second there was significant improvement in the Single Input Processors with wavelength conversion architectures over the Single Input Processor architecture. The packet loss rate for each of the Single Input Processors architectures with wavelength conversion were nearly identical. All of the Single Input Processors archtectures with wavelength conversion are shown with the SIP w/ Four Wavelength Conversion line in Figure 46 because of the nearly identical packet loss rate. All Single Input Processor architectures with wavelength conversion eliminated packet at the output line buffers. The packet loss is eliminated at the outputput line buffers by using a packet contention reduction technique in addition to the output line buffer architecture improvements previously descibed the the Single Input Processor architecture. The packet contention reduction eliminated packet contention at the output line buffers by sending the packets that would cause packet contention from input

Fiber 2 to wavelength converted output lines in output Fiber 1 instead of the non-wavelength converted lines in output Fiber 1. The packet loss rate is even lower for the Parallel Input Processor architecture. The packet loss rate is the lowest of all the architectures shown in Figure 36 from 2.0 gigabits per second for the average transmitter load per line to 10.0 gigabits per second for the average tranmitter load per line. The packet loss rate is the lowest for the Parallel Input Processor architecture because packet loss is reduced at both the forwarding buffers and the output buffers. The Parallel Input Processor architecture has two inprovements to its forwarding buffer archtecture to reduce packet loss. The architecure improvements to the forwarding buffer is to have one forwarding processor per wavelength and one forwarding buffer per wavelength that can delay two packets. The Parallel Input Processor also has the architecure improvement to its output buffer that is described in the Single Input Processor output buffer architecture improvement to reduce packet loss. Wavelength conversion of differnet degrees were added to Single Input Processor architecture and it did not improve the packet loss.

6.8 Average Throughput per Line for Single Input Processor Architecture with Wavelength Conversion

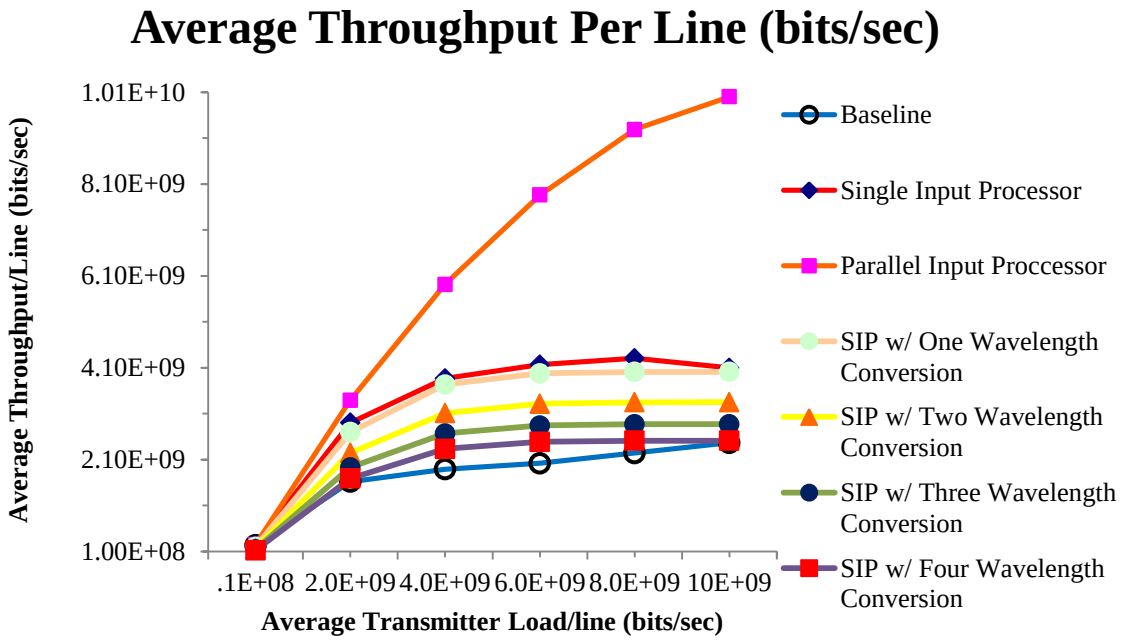

Figure 47 Average Throughput per Line for Baseline, Single Input Processor Architecture with and without Wavelength Conversion, and Parallel Input Processors Architecture

The average throughput per line for the Baseline architecture, Single Input Processor architecture, Parallel Input Processor architecture, Single Input Processor architecture with one, two, three, and four wavelength conversions is shown above in Figure 47. The Baseline architecture has the lowest average throughput per line. The average throughput per line is the lowest for the Baseline architecture because of high packet loss at both the input optical buffer and the output optical buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate

of the proccessor for the fowarding buffer causing packets to overflow the fowarding buffer. The Single Input Processor architecture has higher average throughput per line. This is due to reduced packet loss at the output optical buffer. The Single Input Processor architecture has two improvements to its output buffer to reduce packet loss. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have two additional buffers to delay packets per output fiber. The Single Input Processor with wavelength conversions eliminated packet loss at the output line buffers. The packet loss is eliminated at the outputput line buffers by using a packet contention reduction technique in addition to the output line buffer architecture improvements previously descibed the the Single Input Processor architecture. The packet contention reduction eliminated packet contention at the output line buffers by sending the packets that would cause packet contention from input Fiber 2 to wavelength converted output lines in output Fiber 1 instead of the non-wavelength converted lines in output Fiber 1. The average throughput per line is affected by the number of lines used for wavelength conversion. The average throughput per line is lowered as the number of wavelengths used for wavelength conversion is increased. The reason the average thoughput per line decreased as the number of wavelengths increased is the same amount of input packets was distributed over more output lines. The Single Input Processor architecture had the highest average throughput for the Single Input Processor architectures. The Parallel Input Processors architecture has the highest average throughput per line. The Parallel Input Processors has improvements to its forwarding buffer architecture and its output buffer. This resulted in

reduced packet loss at the forwarding buffer and the output buffers. The reduced packet loss at the buffers resulted in an increase in the average throughput per line. Packet loss was reduced in the forwarding processors by having one forwarding processor per wavelength to forward packets to the output buffer and by having one forwarding buffer per wavelength to delay packets. The eight forwarding processors were able to forward all the incoming packets from the eight input lines into the four output lines. The output buffer of the Parallel Input Processor architecture has the same architecture improvement as the Single Input Processor output buffer. Wavelength conversion of differnet degrees were added to Single Input Processor architecture and it did not improve the packet loss.

6.9 Total Throughput for Single Input Processor Architecture with Wavelength Conversion

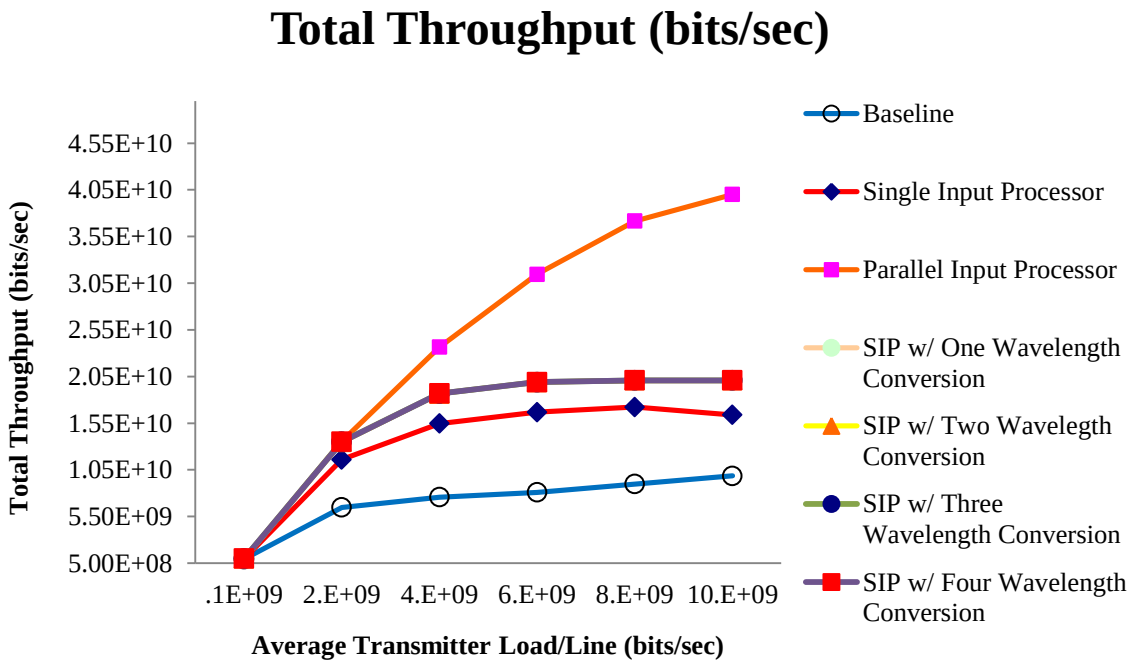

Figure 48 Total Throughput for Baseline, Single Input Processor Architecture with and without Wavelength Conversion, and Parallel Input Processors Architecture

The total throughput for the Baseline architecture, the Single Input Processor architecture, the Parallel Input Processors architecture, the Single Input Processor architecture with one, two, three, and four wavelength conversions is shown above in Figure 48. The Baseline architecture has the lowest total throughput. The total throughput is the lowest for the Baseline architecture because of high packet loss at the input optical buffer and the output optical buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing packets to overflow the forwarding buffer. The Single Input

Processor architecture has higher total throughput than the Baseline architecture due to reduced packet loss at the output optical buffers. The Single Input Processor architecture has two improvements to its output buffer to reduce packet loss. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one output buffer per wavelength. This resulted in two additional buffers to delay packets per output fiber. The Parallel Input Processors architecture has higher total throughput than the Single Input Processor architecture and the Baseline architecture. The higher total throughput is attributed to having one fowarding processor per wavelegth and by having one forwarding buffer per wavelength to delay the incoming packets. The eight forwarding processors were able to forward all incoming packets from eight input lines into four output lines. The total throughput increased about 1 gigabit per second at an average transmitter load per line rate of 10 gigabits per second for the single input processor architectures with wavelength conversion for each additional wavelength is added for wavelength conversion. The Total Throughput is nearly identical for all four single input processor architectures with wavelength conversion for all average transmitter loads per line rates. The Total Throughput for all four single input processor architecture with wavelength conversion is shown in the graph by the Single Input Processor architecture with Four Wavelength Conversion. The three other single input processor architectures with wavelength conversion are underneath the Single Input Processor architecture with Four Wavelength line. Wavelength conversion of differnet degrees were added to Single Input Processor architecture and it did not improve the packet loss.

6.10 Packet Loss Rates for Single and Parallel Input Processors Architectures with and without Next Best Route

The Packet Loss Rate for the Baseline architecture, the Single Input Processor architecture, the Parallel Input Processors architecture, and the Parallel Input Processors architectures with Next Best Route is shown below in Figure 49. As expected the Baseline architecture has the highest packet-loss rate. The packet loss rate is the highest for the Baseline architecture due to high packet loss at the forwarding buffer and the output buffer. Packets are being dropped at the forwarding buffer because packets are being forwarded to the forwarding buffer at a higher rate than forwarding buffer can forward packets and the packets are overflowing the available buffer at the forwarding buffer.

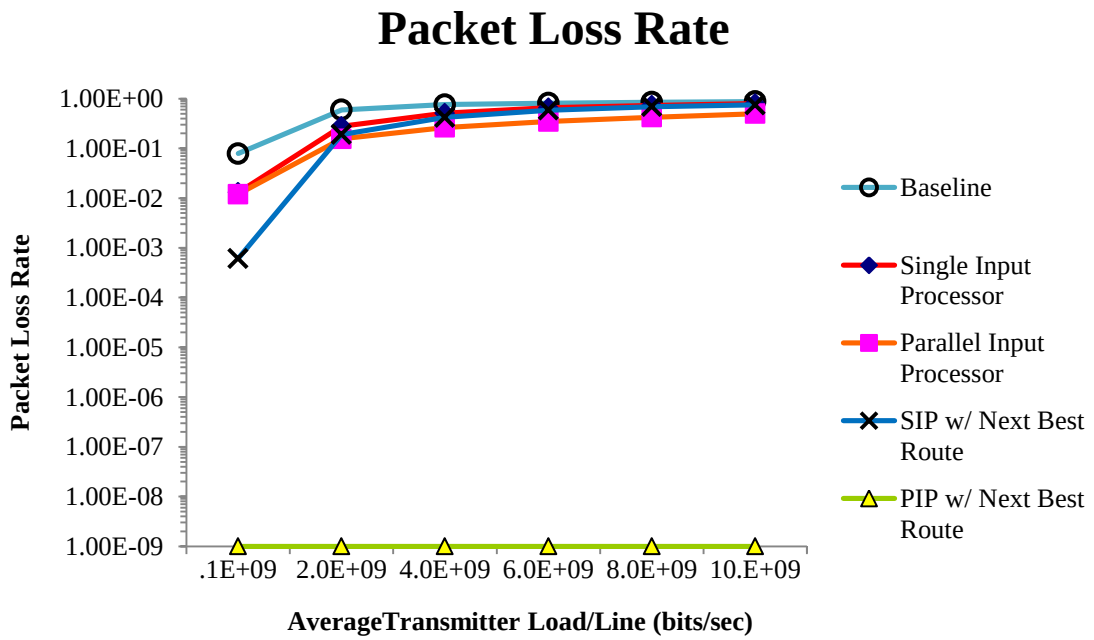

Figure 49 Packet Loss Rates for Baseline, Single and Parallel Input Processors Architectures with and without Next Best Route

The packet loss rate is lower for the Single Input Processor architecture than the Baseline architecture. The packet loss rate is lower because the packet loss at the output optical buffer is lower. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow the forwarding buffer. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one output buffer per wavelength. This resulted in two additional buffers to delay packets per output fiber. The Parallel Input Processor architecture provided improvement to the packet loss rate over the Single Input Processor architecture and the Baseline architecture. The packet loss rate is the lower the Baseline architecture and the Single Input Processor architecture because packet loss is reduced at both the forwarding buffers and the output buffers. The Parallel Input Processor architecture has two inprovements to its forwarding buffer archtecture to reduce packet loss. The architecure improvements is to have one forwarding processor per wavelength and to have one buffer per wavelength that can delay two packets. The Parallel Input Processor also has the architecure improvement to its output buffer that is described in the Single Input Processor output buffer architecture improvement to reduce packet loss. The Parallel Input Processors architecture with Next Best Route has the lowest packet loss rate. The Parallel Input Processors architecture with Next Best Route had the architecture

improvements to its forwarding buffer and output to reduce packet loss as the Parallel Input Processors. The Parallel Input Processors architecture with Next Best Route distributed the traffic from the eight forwarding buffers to eight output line buffers. This traffic redistribution eliminated the packet drop at the output line buffers. The Single Input Processor with Next Route also is not viable. However Parallel Input Processor with Next Best Route did work very well. Hence it can be concluded that multiple input processors are necessary with addition packet contention resolution techniques. This is one of the recommended architecture.

6.11 Average Throughput per Line for Single and Parallel Input Processors Architectures with and without Next Best Route

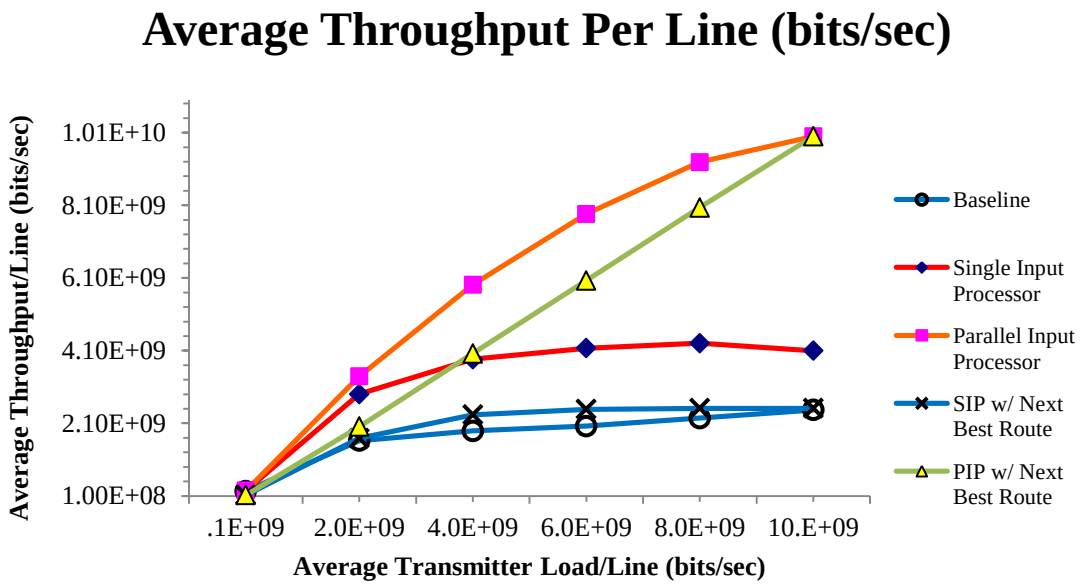

Figure 50 Average Throughput Per Line for Single and Parallel Input Processors Architectures with and without Next Best Route

The average throughput per line for the Baseline architecture, the Single Input Processor architecture, the Parallel Input Processors architecture, and the Parallel Input Processors architecture with Next Best Route is shown above in Figure 50. The Baseline architecture had the lowest average throughput per line for average transmitter load per line of four gigabits per second and higher. This occurred because the Baseline architecture packet loss is high at the forwarding buffer and the output buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow

the forwarding buffer. The Single Input Processor architecture with next Best Route had higher average throughput per line 2.0 gigabits per second for the average transmitter load per line to 10.0 gigabits per second for the average transmitter load per line. The Single Input Processor architecture has higher average throughput per line than the Baseline architecture and the Single Input Processor with Next Best Route. This is due to reduced packet loss at the output buffer. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one buffer per wavelength resulting in an increase of two additional buffers to delay packets per output fiber. The Parallel Input Processors with Next Best Route architecture did not have any packet loss. The average throughput per line reached its theoretical maximum for this architecture. The Parallel Input Processors had the highest average throughput per line. This is because there was a maximum of 80 gigabits per second of traffic being sent to four 10 gigabits per second lines. Even at half the maximum average transmitter load per line, there would be 40 gigabits per second of traffic being sent to four 10 gigabits per second output lines. The output lines are going to be operating at full capacity. In the Parallel Input Processors architecture with Next Best Route, the switch's output lines are only receiving half of the output line's capacity of traffic. At 20 percent of maximum average transmitter load per line, there is four gigabits per second of traffic being sent to each switch output line for the Parallel Input Processor architecture. At the same average transmitter load rate per line in the Parallel Input Processor

architecture with Next Best Route, there are two gigabits per second of traffic sent to each switch output line. The Parallel Input Processor architecture is sending two times the amount of traffic to the switch output lines than the Parallel Input Processor with Next Best Route architecture. Even though the packet drop was much higher in Parallel Input Processors architecture than the Parallel Input Processor architecture with Next Best Route, the average throughput per line is higher in the Parallel Input Processors architecture than the Parallel Processor architecture with Next Best Route. However Parallel Input Processor with Next Best Route did work very well. Hence it can be concluded that multiple input processors are necessary with addition packet contention resolution techniques. This is one of the recommended architecture.

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6.12 Total Throughput for Single and Parallel Input Processors Architectures with and without Next Best Route

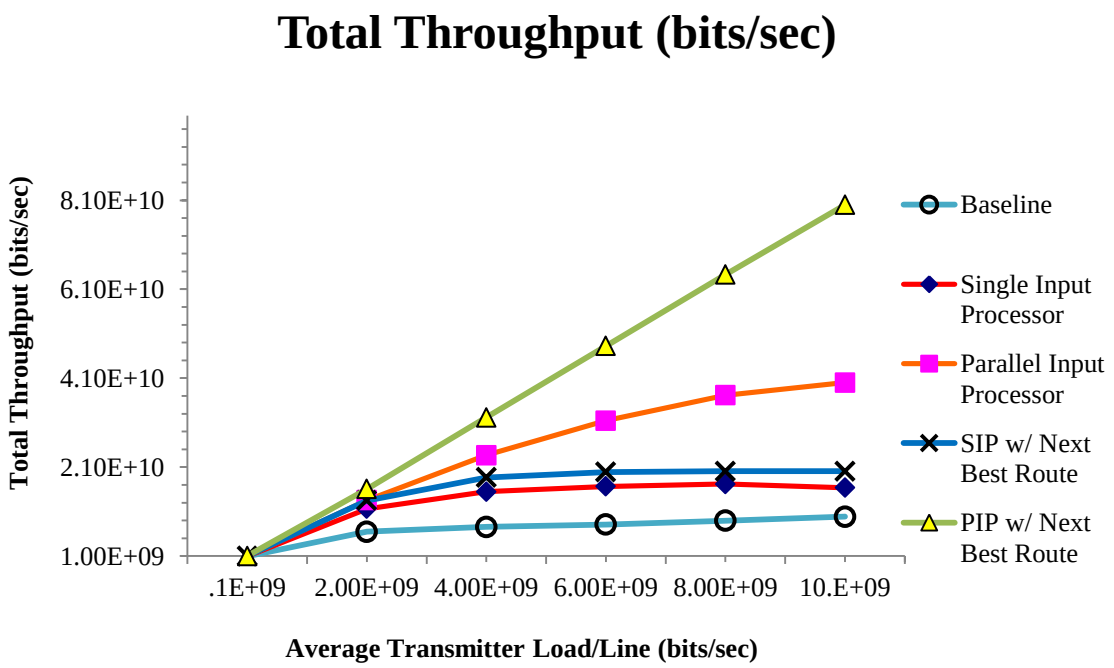

Figure 51 Total Throughput for Baseline, Single and Parallel Input Processors Architectures with and without Next Best Route

The total throughput for the Baseline architecture, the Single Input Processor architecture, the Parallel Input Processors architecture, the Single Input Processor architecture with Next Best Route and the Parallel Input Processors architecture with Next Best Route is shown above in Figure 51. The Baseline architecture has the lowest total throughput. The Baseline architecture has high packet loss at the forwarding buffer and the output buffer. This high packet loss is the reason that the Baseline Architecture has the lowest total throughput. The high packet loss at the forwarding buffer is from having not enough buffer space to delay incoming packets and a single processor with a forwarding rate that is lower than the

incoming packet arrival rate to forward packets to the output. The Parallel Input Processors architecture had no packet loss at the forwarding buffers and higher total throughput than the Baseline architecture, Single Input Processor architecture, and the Single Input Processor architecture with next Best Route. The Parallel Input Processors architecture with Next Best Route had no packet loss at the forwarding buffers and the output buffers. The Parallel Input Processors architecture with Next Best Route has the highest total throughput, because there was not any packet loss at the forwarding buffers or the output buffers. However Parallel Input Processor with Next Best Route did work very well. Hence it can be concluded that multiple input processors are necessary with addition packet contention resolution techniques. This is one of the recommended architecture.

6.13 Packet Loss Rate for Parallel Processors Architectures with Wavelength Conversion

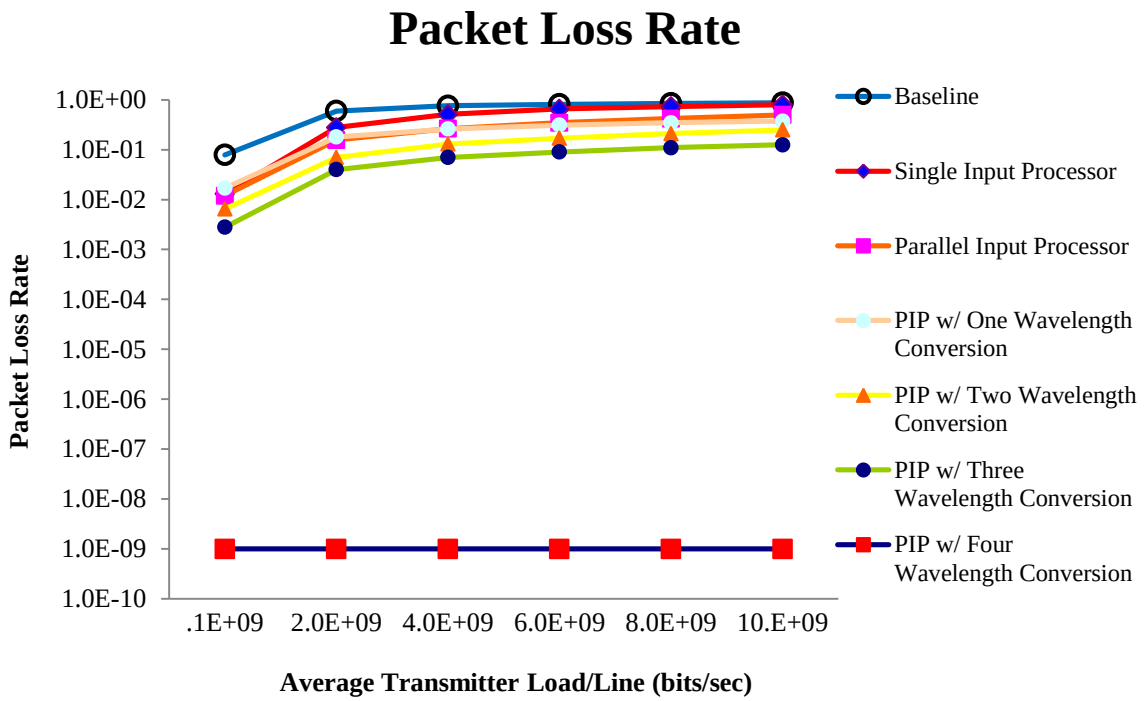

Figure 52 Packet Loss Rates for Baseline, Single Input Processor, and Parallel Processors Architectures with and without Wavelength Conversion

The packet loss rate for the Baseline architecture, the Single Input Processor architecture, the Parallel Input Processors architecture, and the Parallel Input Processors architectures with one, two, three, and four wavelength conversions is shown above in Figure 52. As expected, the Baseline architecture had the highest packet-loss rate. The Baseline architecture has high packet loss at the forwarding buffer and the output buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow

the forwarding buffer. The packet loss rate is lower for the Single Input Processor architecture than the Baseline architecture. The packet loss rate is lower because the packet loss at the output optical buffer is lower. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss. The first improvement to the output buffer architecture is to have one output per wavelength. The second improvement is to have one processor per wavelength to forward packets to the next switch or network device. This improvement resulted in having two additional buffers to delay packets at each output fiber. The Parallel Input Processors architecture with One Wavelength Conversion and the Parallel Input Processors architecture had the next lowest packet-loss rate. The Parallel Input Processor architecture packet-loss rate is slightly lower than the Parallel Input Processors architecture with One Wavelength Conversion at low average transmitter load per line rates. The Parallel Input Processors architecture with One Wavelength Conversion has slightly lower packet-loss rate at higher average transmitter load per line rates. The packet-loss rate is relatively high for the Parallel Input Processors architecture with One Wavelength Conversion because the four wavelengths from fiber two are sent to one wavelength on Fiber 1. The incoming packet rate to wavelength converted output buffer on Fiber 1 is higher than the forwarding rate of the output buffer's processor. In the Parallel Input Processors architecture, packets are dropped at output Fiber 1's output buffers. The packet-loss rate for the Parallel Input Processors architecture with Two Wavelength and Three Wavelength Conversion is slightly lower than the previously described architectures. Still, the packet-loss rate is relatively high. The Parallel Input

Processors architecture with Four Wavelength Conversion shows a much improved packet loss rate. This architecture had no packet loss. In this architecture the incoming packet rate to the wavelength converted output buffers never exceed the output buffer's processors forwarding rate. From the results it is shown that parallel input processor with number of wavelength conversion less than number of incoming wavelengths results did provide good performance. However Parallel Input Processor with a number of wavelength converters equal to the number of incoming wavelengths did provide very good performance. Hence this is a recommended architecture.

6.14 Average Throughput per Line for Parallel Input Processors Architecture with Wavelength Conversion

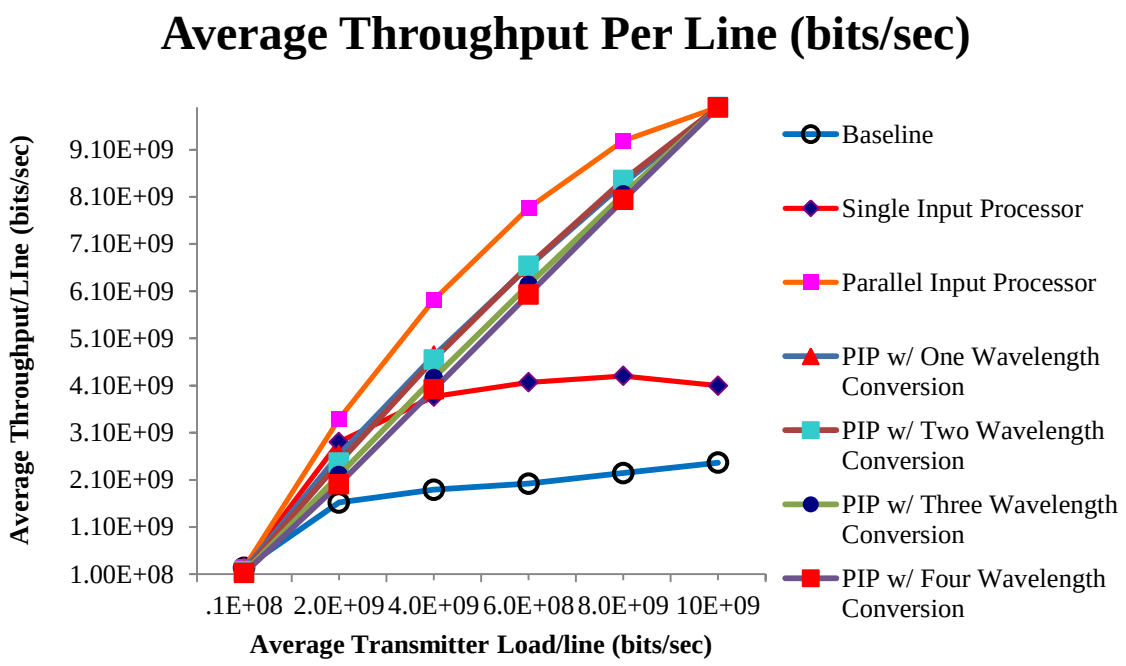

Figure 53 Average Throughput per Line for Baseline, Single Input Processor, and Parallel Input Processors Architecture with and without Wavelength Conversion

The average throughput per line for the Baseline architecture, the Single Input Processor architecture, Parallel Input Processors architecture, and the Parallel Input Processors architecture with one, two, three, and four wavelength conversions are shown above in Figure 53. The Baseline architecture had the lowest average throughput per line because its packet loss rate is the highest of the architectures shown. The Single Input Processor architecture has higher average throughput per line than the Baseline architecture. This is due to reduced packet loss at the output buffer. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss. The first

improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one buffer per wavelength resulting in an increase of two additional buffers to delay packets per output fiber. The Parallel Input Processors architecture with One Wavelength Conversion and the Parallel Input Processors architecture with Two Wavelength Conversion architectures have the next highest average throughput per line. In these architectures, the traffic from input Fiber 1 is sent to output Fiber 1. There is no increase in the average throughput per line on the output lines on output Fiber 1 used for the switch's input Fiber 1 input lines. It is the traffic from input Fiber 2 that causes the increase in the average throughput per line. In the Parallel Input Processors architecture with One Wavelength Conversion, the four input lines from input Fiber 2 are sent to one wavelength conversion output line on output Fiber 1. The wavelength converted output line is going to reach capacity at the lowest average transmitter load per line. There is going to be one switch output line with a higher throughput than the other four output lines receiving traffic from Fiber 1 input lines. In the Parallel Input Processors architecture with Two Wavelength Conversion, there are going to be two output lines with higher average throughput per line. Each of the two wavelength converted output lines is going to receive half as much traffic as in the Parallel Input Processors architecture with One Wavelength Conversion and twice as much traffic as the non-wavelength converted switch output lines. On the Parallel Input Processors architecture with Two Wavelength Conversion, there are two output lines with higher average throughput per lines. The Parallel Input Processors architecture had the highest average throughput per line. The Parallel Input Processors has

improvements to its forwarding buffer architecture and its output buffer to reduce packet loss and to increase the average throughput per line. Packet loss was reduced in the forwarding processors by having one forwarding processor per wavelength to forward packets to the output buffer and by having one forwarding buffer per wavelength to delay packets. The eight forwarding processors were able to forward all the incoming packets from the eight input lines into the four output lines. The output buffer of the Parallel Input Processor architecture has the same architecture improvement as the Single Input Processor output buffer. From the results it is shown that parallel input processor with number of wavelength conversion less than number of incoming wavelengths results did provide good performance. However Parallel Input Processor with a number of wavelength converters equal to the number of incoming wavelengths did provide very good performance. Hence this is a recommended architecture.

6.15 Total Throughput for Parallel Input Processors with Wavelength Conversion

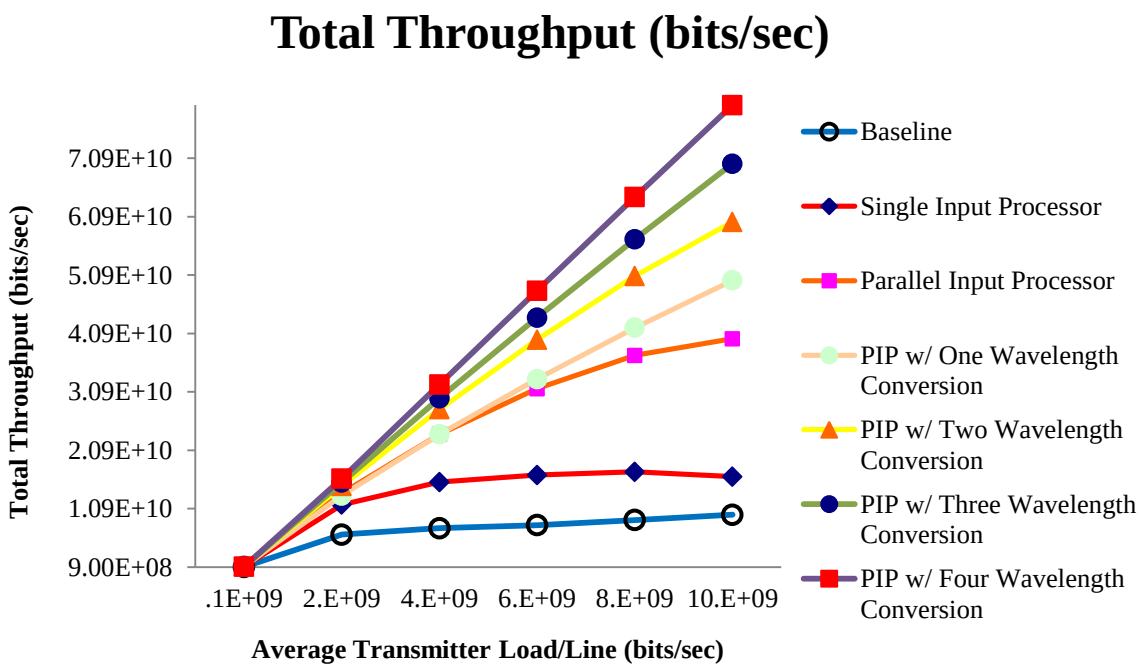

Figure 54 Total Throughput for Baseline, Single Input Processor, and Parallel Input Processors with and without Wavelength Conversion

The total throughput for the Baseline architecture, the Single Input Processor architecture, the Parallel Input Processors architecture, and the Parallel Input Processors architecture with one, two, three, and four wavelength conversions is shown above in Figure 54. The Baseline architecture has the highest packet loss and has the lowest total throughput because of the high packet loss. The Baseline architecture has high packet loss at the forwarding buffer and the output buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the

fowarding buffer causing packets to overflow the fowarding buffer. The packet loss at the output buffer is from incoming packets arriving at a higher rate from the forwarding buffer of input Fiber 1 and input Fiber 2 to the output buffer than the forwarding rate of the proccessor for the output buffer causing packets to overflow the output buffer. The Single Input Processor architecture has higher average throughput per line. This is due to reduced packet loss at the output optical buffer. The Single Input Processor architecture has two improvements to its output buffer to reduce packet loss. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have two additional buffers to delay packets per output fiber. The Parallel Input Processors architecture had lower packet loss and higher total throughput than the Baseline architecture and the Single Input Processor architecture. The higher total throughput is attributed reduced packet loss at the forwarding buffer and the output buffer. Packet loss at the forwarding buffer is reduced by having one forwarding processor per wavelength to forward packets to the output buffer and by having one forwarding buffer per wavelength to delay the incoming packets. The eight processors at the forwarding buffers were able to forward all incoming packets from eight input lines into four output lines. All the Parallel Input Processors architectures with wavelength conversion had similar results for two gigabits per second and below for the average transmitter load per line. At ten gigabits per second per for the average transmitter load per line, there was an increase of about one gigabit for the total throughput when a wavelength was added for wavelength conversion. From the results it is shown that parallel input processor with number of wavelength

conversion less than number of incoming wavelengths results did provide good performance. However Parallel Input Processor with a number of wavelength converters equal to the number of incoming wavelengths did provide very good performance. Hence this is a recommended architecture.

6.16 Packet Loss Rate for Parallel Input Processor Architecture with Four Wavelength Conversion

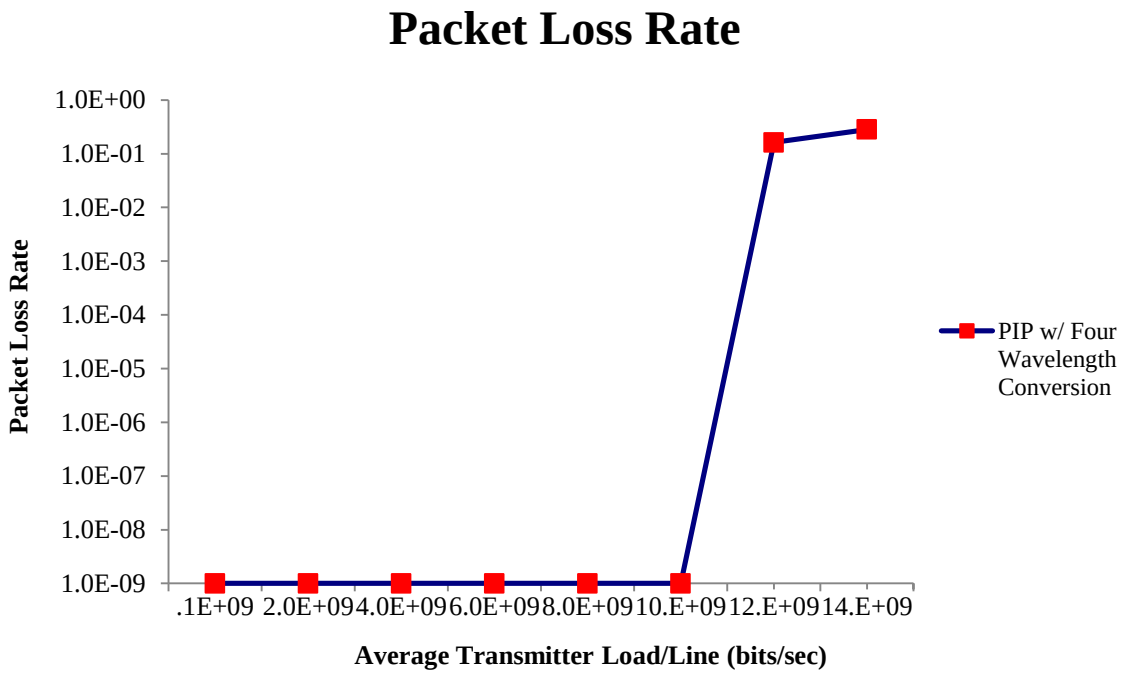

Figure 55 Packet Loss Rate for Parallel Input Processor Architecture with Four Wavelength Conversion

The packet loss rate for Parallel Input Processor architecture with Four Wavelength Conversion is shown above in Figure 55. There is no packet loss at the forwarding buffers and output buffers for average transmitter load per line rates up to 10 gigabits per second. The Parallel Input Processor architecture has two inprovements to its forwarding buffer archtecture to reduce packet loss. The architecure improvements to the forward buffer is to have one forwarding processor per wavelength and one forwarding buffer per wavelength that can delay two packets. The packet loss at the output buffers in output Fiber 1 was eliminated for all average transmitter load per line rates by sending the packets coming from

input Fiber 2's forwarding buffer to the four wavelength converted lines in output Fiber 1. Packet loss occurs at the forwarding buffer for average transmitter load per line rates above 10 gigabits per second. The packet loss is from packets overflowing the forwarding buffer. Packet loss is from having packets arriving at the forwarding buffers at a higher rate than the forwarding rate of the forwarding processor can forward packets to the output buffers. The Parallel Input Processor with Four Wavelength Conversion will work only if the input data rate is less than or equal to the processing rate of the individual input processor. If the input rate goes above the processing speed of the individual processors and then the performance goes down. Thus the input line with higher data rate can be accommodated if input processors or with correspondingly higher power processing speed are available.

6.17 Average Throughput per Line for Parallel Input Processor Architecture with Four Wavelength Conversion

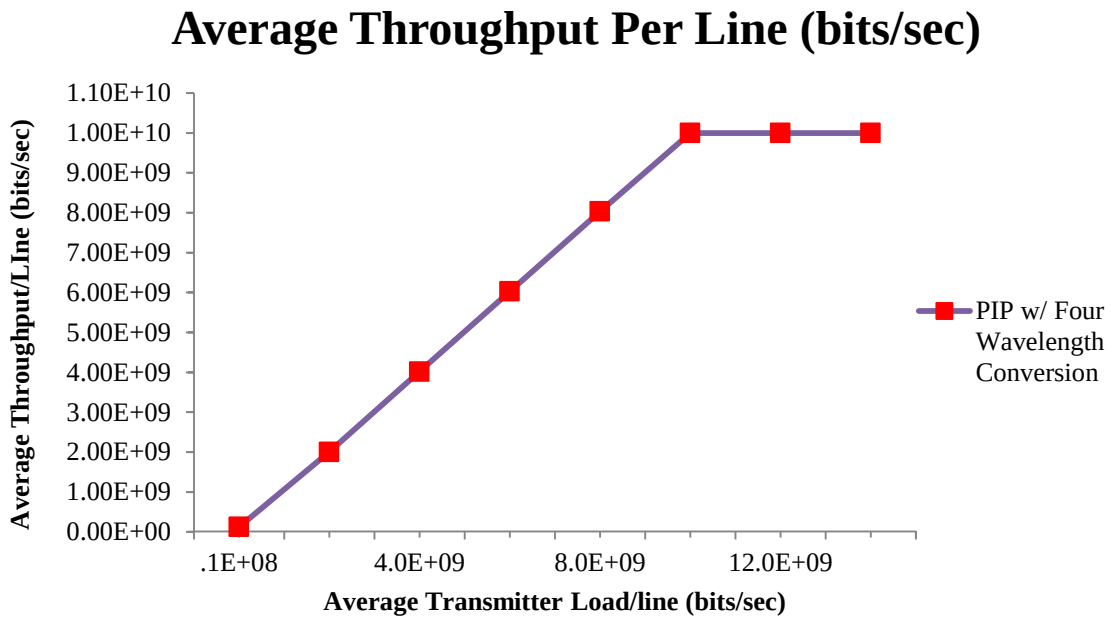

Figure 56 Average Throughput Per Line for Parallel Input Processor Architecture with Four Wavelength Conversion

The average throughput per line for Parallel Input Processor architecture with Four Wavelength Conversion is shown above in Figure 56. The average throughput per line is equal to the average transmitter per line from 0.1 gigabits per second for the average transmitter load per line up to 10 gigabits per second for the average transmitter per line. There are several reasons why the average throughput per line was equal to the average transmitter per load. The first reason was the number of input lines was equal to the output lines. The second reason was packet drop was eliminated in both the forwarding buffers and the output line buffers. Packet loss is elimnated in the forwarding processors by having one

forwarding processor per wavelength to forward packets to the output buffers and by having one forwarding buffer per wavelength to delay packets. The packet loss is eliminated at the outputput line buffers by using a packet contention reduction technique in addition to the output line buffer architecture improvements previously descibed the the Single Input Processor architecture. The packet contention reduction eliminated packet contention at the output line buffers by sending the packets that would cause packet contention from input Fiber 2 to wavelength converted output lines in output Fiber 1 instead of the non-wavelength converted lines in output Fiber 1. The eight forwarding processors were able to forward all the incoming packets from the eight input lines into the four output lines on output Fiber 1. The average throughput per line peaks at 10 gigabits per second for average transmitter load per line of 10 gigabits per second to 14 gigabits per second. The average throughput per line reaches a maximum at 10 gigabits per second because packets overflow the forwarding buffer when incoming packets to the forwarding buffers exceed the rate of 10 gigabits per second. The forwarding rate of the forwarding processor for the forwarding buffers is 10 gigabits per second. The Parallel Input Processor with Four Wavelength Conversion will work only if the input data rate is less than or equal to the processing rate of the individual input processor. If the input rate goes above the processing speed of the individual processors and then the performance goes down. Thus the input line with higher data rate can be accommodated if input processors or with correspondingly higher power processing speed are available.

6.18 Total Throughput for Parallel Input Processor Architecture with Four Wavelength Conversion

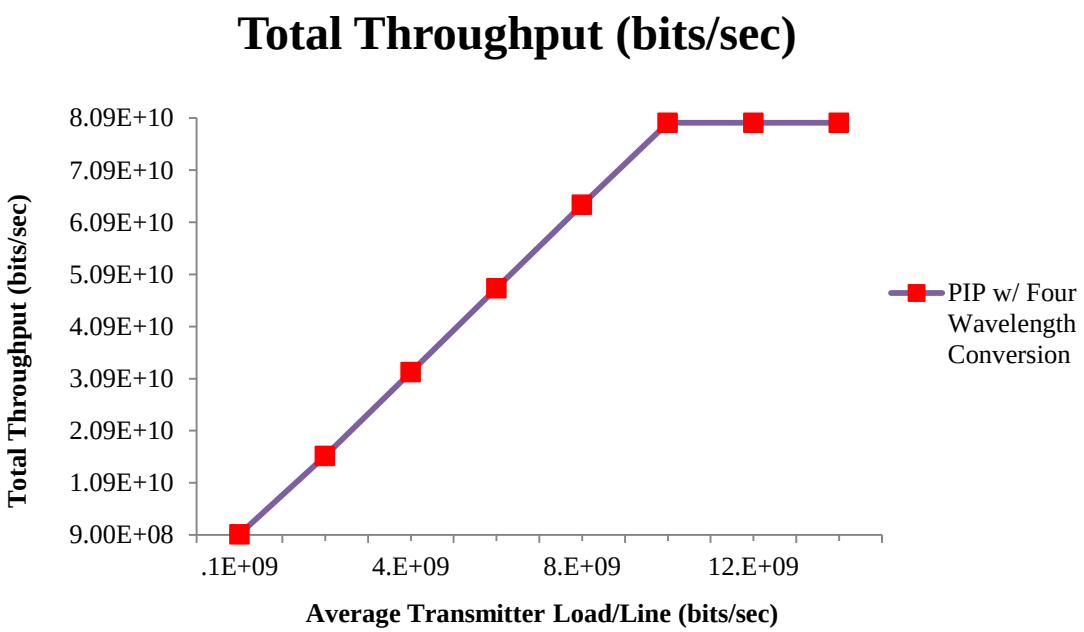

Figure 57 Total Throughput for Parallel Input Processor Architecture with Four Wavelength Conversion

The total throughput for Parallel Input Processor architecture with Four Wavelength Conversion is shown above in Figure 57. The total throughput is equal to the total amount of packets in bits per second that is sent from all eight input sources to the switch up to average transmitter load per lines of 10 gigabits per second. This occurred because there was no packet drop at both the forwarding buffers and all output line buffers for average transmitter load per line rates up to 10 gigabits per second. Packet loss is elimnated in the forwarding processors by having one forwarding processor per wavelength to forward packets to the output buffers and by having one forwarding buffer per wavelength to delay packets. The

packet loss is eliminated at the outputput line buffers by using a packet contention reduction technique in addition to the output line buffer architecture improvements previously descibed the the Single Input Processor architecture. The packet contention reduction eliminated packet contention at the output line buffers by sending the packets that would cause packet contention from input Fiber 2 to wavelength converted output lines in output Fiber 1 instead of the non-wavelength converted lines in output Fiber 1. The total throughput is flat for average transmitter load per line rates of 10 gigabits per second to 14 gigabits per second. The total throughput is flat because the average throughput per line is constant for average transmitter load per line rates of 10 gigabits per second to 14 gigabits per second. The average throughput per line reaches a maximum at 10 gigabits per second because packets overflow the forwarding buffer when incoming packets to the forwarding buffers exceed the rate of 10 gigabits per second. The Parallel Input Processor with Four Wavelength Conversion will work only if the input data rate is less than or equal to the processing rate of the individual input processor. If the input rate goes above the processing speed of the individual processors and then the performance goes down. Thus the input line with higher data rate can be accommodated if input processors or with correspondingly higher power processing speed are available.

6.19 Packet Loss Rate for Single and Parallel Input Processors Architectures with Four Wavelength Conversion

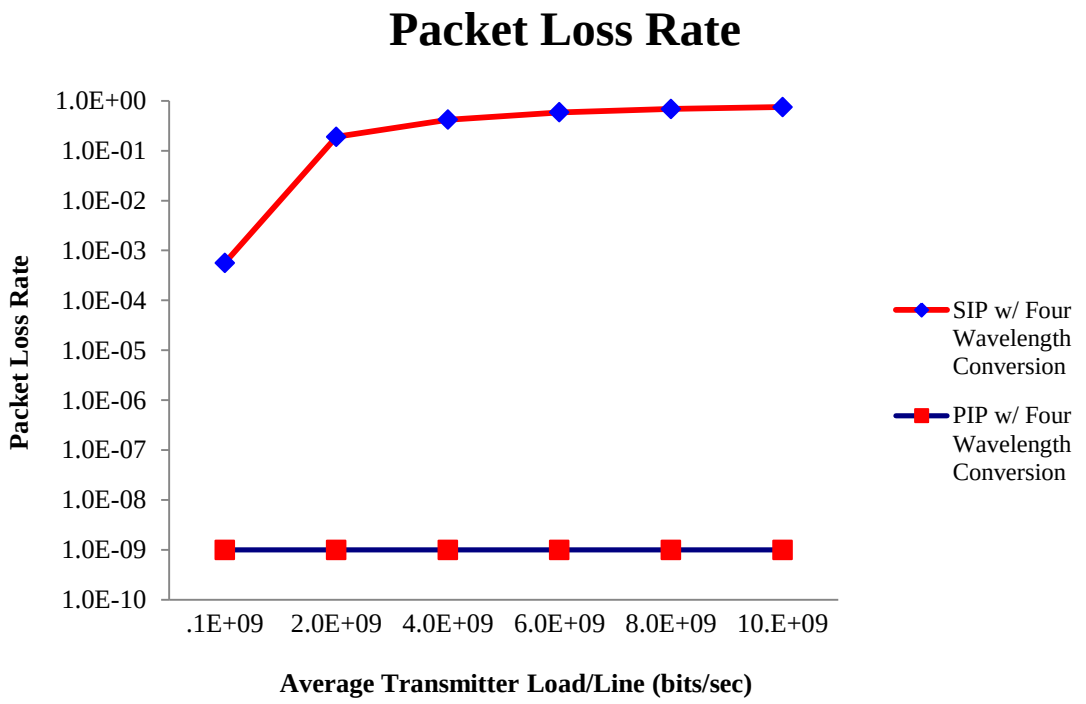

Figure 58 Packet Loss Rate for Single and Parallel Input Processors Architectures with Four Wavelength Conversion

The packet loss rate for the Single and the Parallel Input Processors architectures with Four Wavelength Conversion is shown above in Figure 58. The Single Input Processor architecture with Four Wavelength Conversion has packet loss at the forwarding buffer and does not have any packet loss at the output buffers. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow

the forwarding buffer. The packet loss at the output buffers in output Fiber 1 was eliminated by sending the packets coming from input Fiber 2's forwarding buffer to the four wavelength converted lines in output Fiber 1. The Parallel Input Processor architecture with Four Wavelength Conversion does not have any packet loss at the forwarding and output buffers. The Parallel Input Processor architecture has two inprovements to its forwarding buffer archtecture to reduce packet loss. The architecure improvements to the forwarding buffer is to have one forwarding processor per wavelength and one forwarding buffer per wavelength that can delay two packets. The packet loss at the output buffers in output Fiber 1 was eliminated by sending the packets coming from input Fiber 2's forwarding buffer to the four wavelength converted lines in output Fiber 1. The Single Input Processor architecture evan with a number of wavelength converters equal to the number of incoming wavelengths does perform satisfactorly. However in the case of Parallel Input Processors archtecture with the number of processors equal to the number of incoming lines and the number of wavelength converters equal to the number of incoming wavelengths performs very well. Hence this is one of the recommended architectures.

6.20 Average Throughput for Single and Parallel Input Processors Architectures with Four Wavelength Conversion

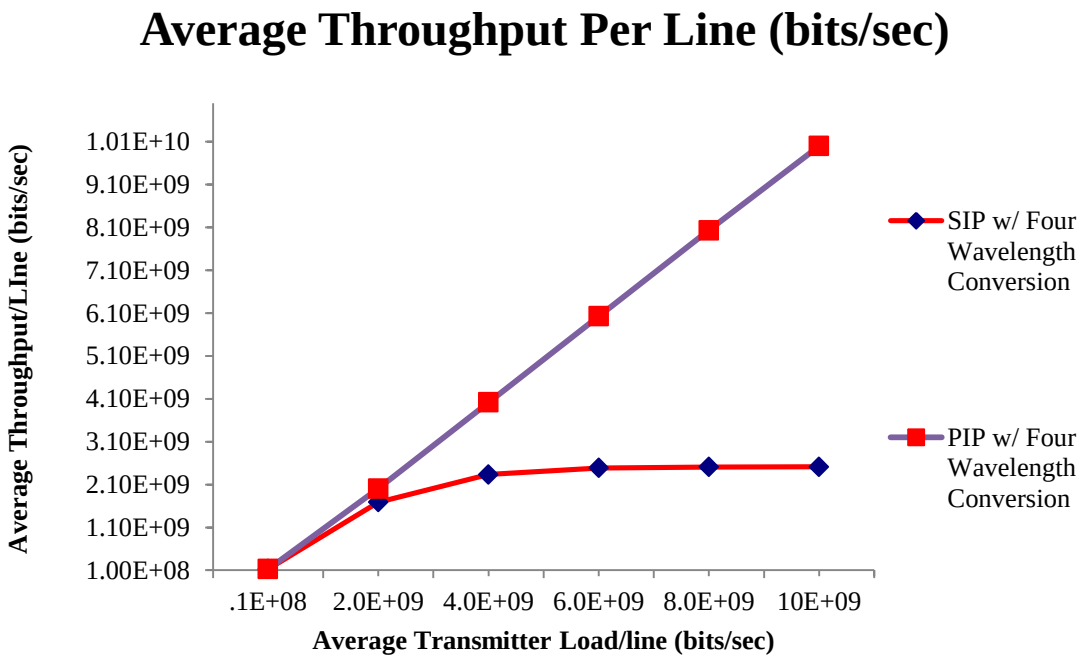

Figure 59 Average Throughput for Single and Parallel Input Processors Architectures with Wavelength Conversion

The average throughput for Single and Parallel Input Processors architectures with Four Wavelength Conversion is shown above in Figure 59. The average throughput per line peaks at 2.5 gigabits per second for the Single Input Processor architecture with Four Wavelength Conversion. The single processor with a forwarding speed of 10 gigabits per second limits the maximum average throughput per line to 2.5 gigabits per second. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss and increase the average throughput per line. The first improvement is to have

one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one buffer per wavelength resulting in an increase of two additional buffers to delay packets per output fiber. Packet loss is eliminationed at the outputs by sending packets from Fiber 2's four forwarding buffers to the four wavelength converted output lines in output Fiber 1. This final reduction of packet loss at the output buffers allows the average throughput per to reach its maximum of 2.5 gigabits per second. The Parallel Input Processor architecture with Four Wavelength Conversion can forward packets at the input average transmitter load per line rate up to 10 gigabits per second. Two improvements to the forwarding buffer allows packets to be forwarded at rates up 10 gigabits per second. The first improvement to the forwarding buffer is to have one forwarding processor per wavelength to forward packets to the output buffers. The second improvement is to have one forwarding buffer per wavelength to delay packets. This helped to reduce packet loss and increase the average throughput per line. The output buffer of the Parallel Input Processor architecture has the same architecture improvement as the Single Input Processor output buffer. There is one buffer per output line and one processor per output line to forward packets. Packet loss is eliminationed at the output buffers by sending packets from input Fiber 2's four forwarding buffers to the four wavelength converted output lines in output Fiber 1. The Single Input Processor architecture evan with a number of wavelength converters equal to the number of incoming wavelengths does perform satisfactorly. However in the case of Parallel Input Processors archtecture with the number of processors equal to the number of incoming lines and the number of wavelength converters equal to the

number of incoming wavelengths performs very well. Hence this is one of the recommended architectures.

6.21 Total Throughtput for Single and Parallel Input Processors Architectures with Four Wavelength Conversion

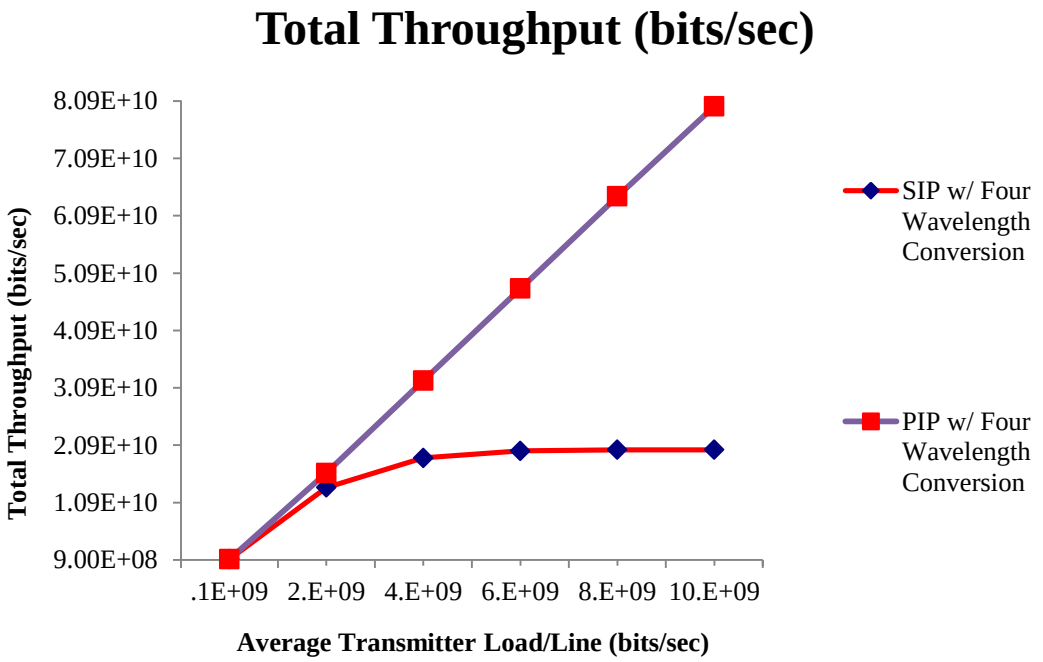

Figure 60 Total Throughput for Single and Parallel Input Processors Architectures with Four Wavelength Conversion

The total throughput for Single and Parallel Input Processors architectures with Four Wavelength Conversion is shown above in Figure 60. The total throughput for the Single Input Processor architecture with Four Wavelength Conversion peaks at 20 gigabits per second. The average throughput per line is about 2.5 gigabits per second. There is eight output lines. The expected value for the total throughput for the Single Input Processor with Four Wavelength Conversions would be 20 gigabits per second. The total throughput for the Parallel Input Processors architecture with Four Wavelength Conversion is equal to the total

amount of packets in bits per second that is sent from all input sources to the switch. This is what is expected for total throughput for the Parallel Input Processors architecture with Four Wavelength Conversions. The Parallel Input Processors architecture with Four Wavelength Conversions forwards all packets and eliminates all packet loss. The Single Input Processor architecture evan with a number of wavelength converters equal to the number of incoming wavelengths does perform satisfactorly. However in the case of Parallel Input Processors archtecture with the number of processors equal to the number of incoming lines and the number of wavelength converters equal to the number of incoming wavelengths performs very well. Hence this is one of the recommended architectures.

6.22 Queuing Delay Results

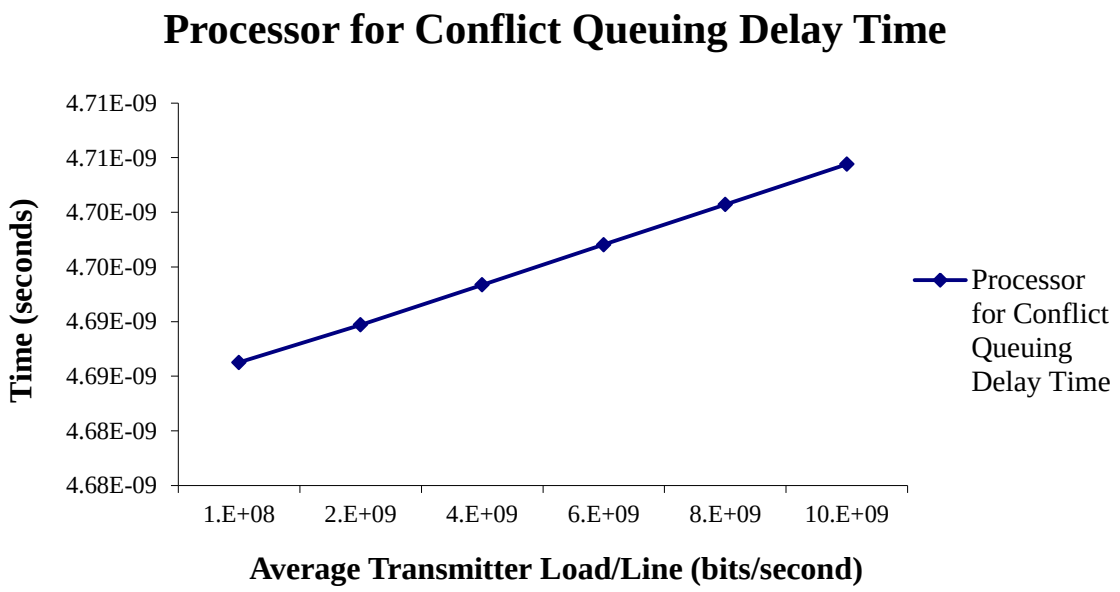

Figure 61 Queuing Time Delay for Processor for Conflict

The queuing time delay for Processor for Conflict is shown above in Figure 61. The lookup processor from an IEEE paper could perform 213.4 mega-lookups per second. Each lookup had an average service time of 4 nanoseconds. This service time was used for the analysis. The analysis assumed 512 processors are to access the routing table. The service rate, inversely proportional to the service time, is 0.213 giga-lookups per second. The queuing time delay was calculated for a M/M/1 queue.

6.23 Packet Loss Rate for Unified Architecture and Parallel Input Processor Architecture with Four Wavelength Conversion

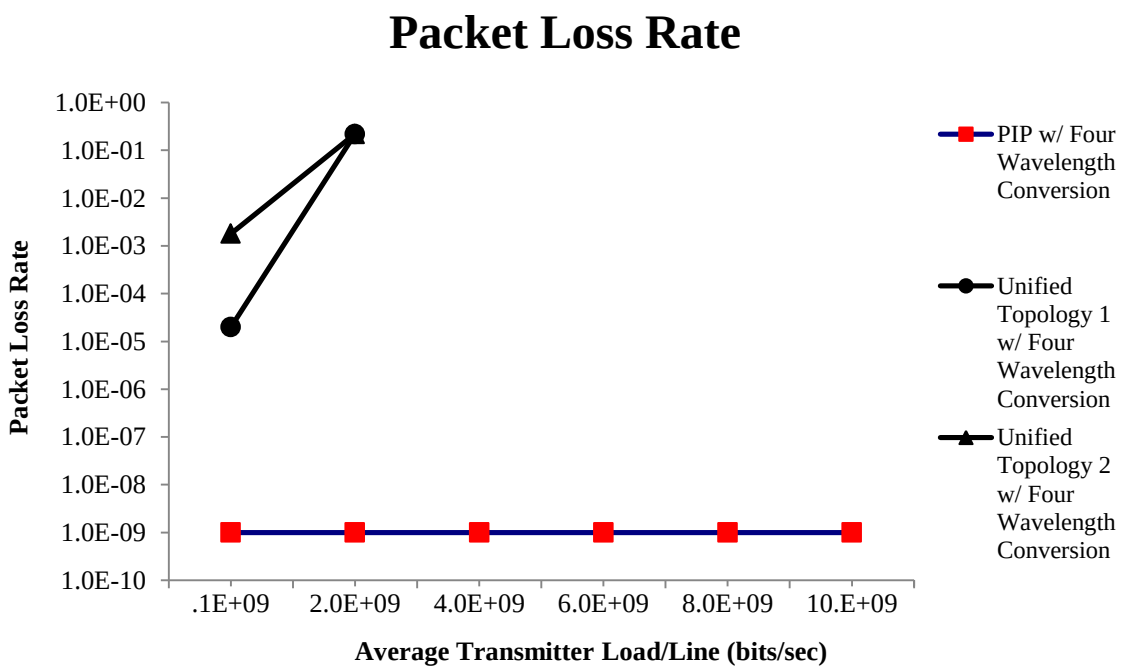

Figure 62 Packet Loss Rates for Unified Architecture and Parallel Input Processor Architecture with Four Wavelength Conversion

The packet loss rate for Parallel Input Processors architecture with Four Wavelength Conversion, Unified Topology 1 with Four Wavelength Conversion, and Unified Topology 2 with Four Wavelength Conversion is shown above in Figure 62. The packet loss rate for the Unified Study Topology 1 and Topology 2 is higher than the Parallel Input Processor architecture with Four Wavelength Conversion. The packet loss rate for the Unified Topology 1 with Four Wavelength Conversions and Unified Topology 2 with Four Wavelength Conversion peaked 0.5 at an average transmitter load per line rate of 2.0 gigabits

per second. The Parallel Input Processors architecture with Four Wavelength Conversion has no packet loss to an average transmitter load per line rate of 10 gigabits per second.

6.24 Network Throughput for Unified Architecture with Four Wavelength Conversion and Average Throughput for Parallel Input Processors Architecture with Four Wavelength Conversion

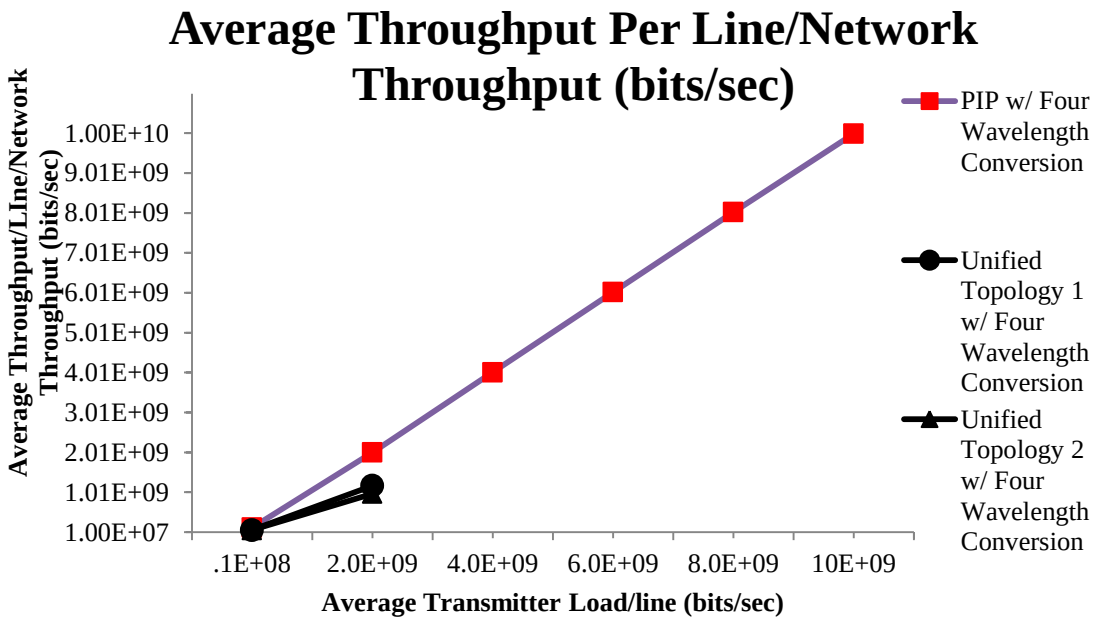

Figure 63 Network Throughput for Unified Architecture with Four Wavelength Conversion Average Throughput Per Line for Parallel Processors Architecture with Four Wavelength Conversion

The network throughput for Unified architecture with Four Wavelength Conversion for Topology 1 and Topology 2, and the average throughput per line for Parallel Input Processors architecture with Four Wavelength Conversion are shown above in Figure 63.

The network throughput for the Unified Topology 1 with Four Wavelength Conversion is 62.5 megabits per second for an average transmitter load per line of 0.1 gigabits per second.

The network throughput for the Unified Topology 2 with Four Wavelength Conversion is 62.6 megabits per second for an average transmitter load per line of 0.1 gigabits per second.

The average throughput for the Parallel Input Processors architecture with Four Wavelength Conversion is 100 megabits per second for an average transmitter load per line rate of 0.1 gigabits per second. The network throughput for the Unified Topology 1 with Four Wavelength Conversion reaches its maximum at 1.2 gigabits per second at an average transmitter load per line of 2.0 gigabits per second. The network throughput for the Unified Topology 2 with Four Wavelength Conversion reaches its maximum at 0.98 gigabits per second at an average transmitter load per line of 2.0 gigabits per second. The average throughput for the Parallel Input Processor architecture with Four Wavelength Conversion is 2.0 gigabits per second at an average transmitter load per line rate of 2.0 gigabits per second. The average throughput per line for the Parallel Input Processors architecture with Four Wavelength Conversion reaches its maximum at 10 gigabits per second at an average transmitter load per line rate of 10 gigabits per second. The average throughput for Parallel Input Processor architecture with Four Wavelength Conversion is higher than the network throughput for the Unified Topology 1 with Four Wavelength Conversion and Unified Topology 2 with Four Wavelength Conversion from an average transmitter load per line rate of 0.1 gigabits per second to 10 gigabits per second.

Chapter 7 Results for Single Packet Output Buffer Size vs. Two Packet Output Buffer Size

7.1 Packet Loss Rate for Single and Parallel Input Processors Architectures with One Packet and Two Packet Output Buffers Sizes

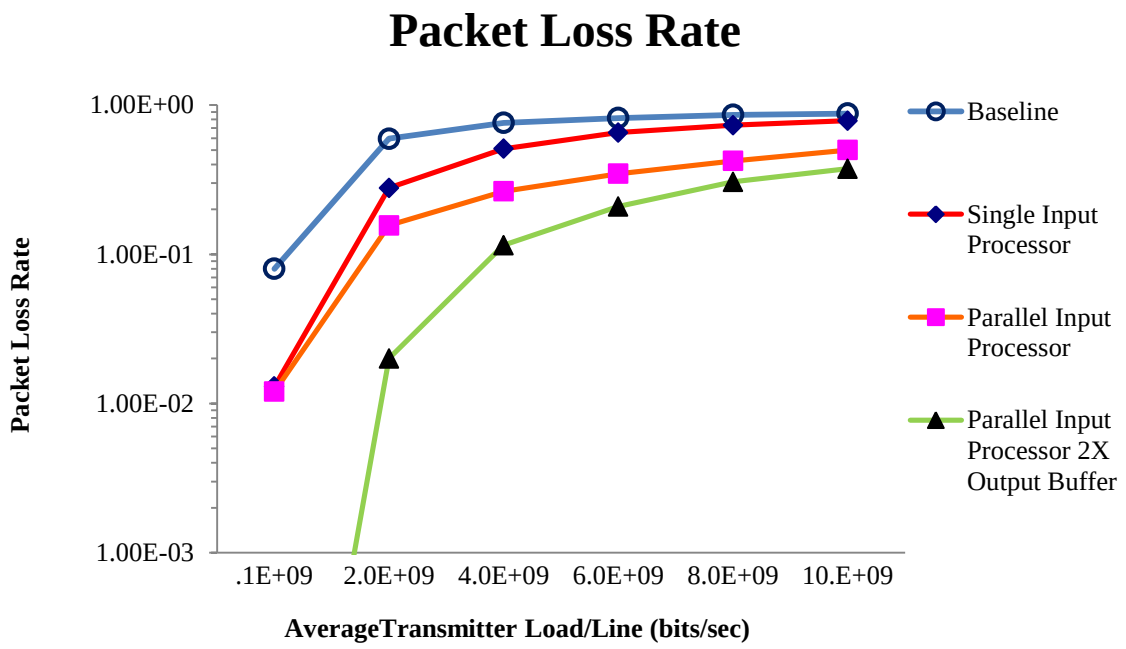

Figure 64 Packet Loss Rate for Single and Parallel Input Processors Architectures with One Packet and Two Packet Output Buffer Sizes

The packet loss rate for the Baseline architecture, Single Input Processor architecture, Parallel Input Processors architecture, and Parallel Input Processor architecture with Two Packet Output Buffer is shown above in Figure 64. The packet loss rate is the highest for the Baseline architecture due to high packet loss at the forwarding buffer and the output buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the forwarding rate of the proccessor for the

fowarding buffer causing the packets to overflow the forwarding buffer. The packet loss rate is lower for the Single Input Processor architecture than the Baseline architecture. The packet loss rate is lower because the packet loss at the output buffer is lower. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss. The first improvement to the output buffer architecture is to have one output buffer per wavelength. The second improvement is to have one processor per wavelength to forward packets to the next switch or network device. This improvement resulted in having two additional buffers to delay packets at each output fiber. The packet loss rate is even lower for the Parallel Input Processor architecture. The packet loss rate is the lower than the Baseline architecture and the Single Input Processor architecture because packet loss is reduced at both the forwarding buffers and the output buffers. The Parallel Input Processor architecture has two inprovements to its forwarding buffer/processor archtecture to reduce packet loss. The architecure improvements to the forward buffer is to have one forwarding processor per wavelength and one forwarding buffer per wavelength that can delay two packets. The Parallel Input Processor also has the architecure improvement to its output buffer that is described in the Single Input Processor output buffer architecture improvement to reduce packet loss. The packet loss rate for the Parallel Input Processor with Two Packet Output Buffer had the lowest packet loss rate. The larger output buffer size helped reduce packet loss at the output buffers.

7.2 Average Throughput per Line for Single and Parallel Input Processors Architectures with One Packet and Two Packet Output Buffer Sizes

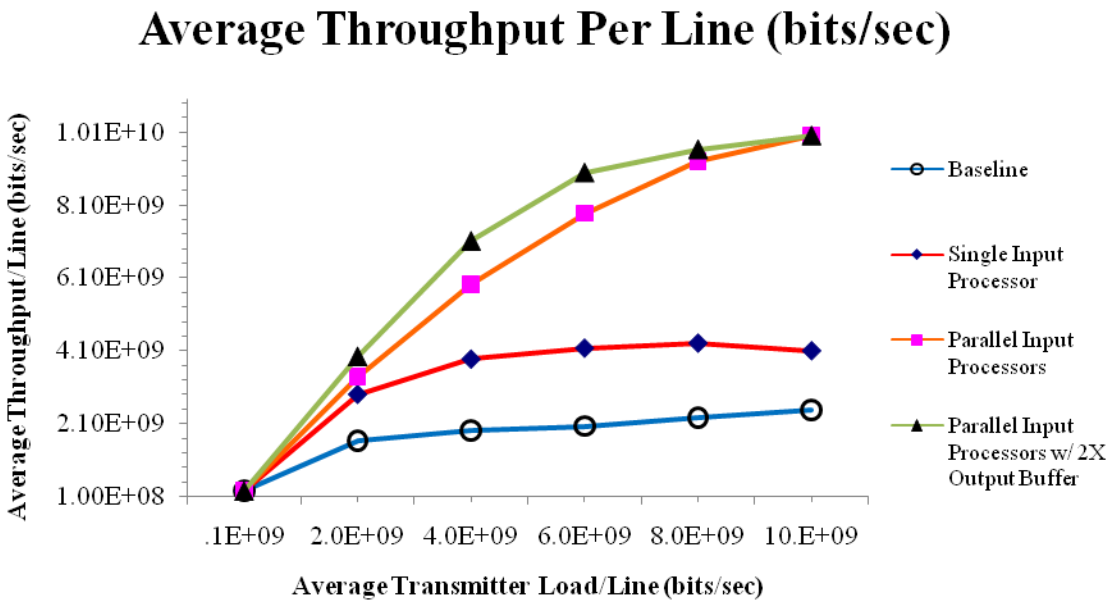

Figure 65 Average Throughput per Line for Single and Parallel Input Processors Architectures with One Packet and Packet Output Buffer Sizes

The average throughput per line for the Baseline architecture, Single Input Processor architecture, the Parallel Input Processors architecture, and the Parallel Input Processors architecture with Two Packet Output Buffer is shown above in Figure 65. The Baseline architecture has the lowest Average Throughput per line. The average throughput per line is the lowest for the Baseline architecture because of high packet loss at both the forwarding buffer and the output buffer. The Single Input Processor architecture has higher average throughput per line than the Baseline architecture. This is due to reduced packet loss at the output buffer. The Single Input Processor architecture has two improvements to its output buffer architecture to reduce packet loss. The first

improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one buffer per wavelength resulting in an increase of two additional buffers to delay packets per output fiber. The Parallel Input Processors architecture has higher average throughput per line than the Baseline architecture and the Single Input Processor architecture. The Parallel Input Processors has improvements to its forwarding buffer architecture and its output buffer to reduce packet loss and to increase the average throughput per line. Packet loss was reduced in the forwarding processors by having one forwarding processor per wavelength to forward packets to the output buffer and by having one forwarding buffer per wavelength to delay packets. The eight forwarding processors at each forwarding buffer were able to forward all the incoming packets from the eight packet sources into the four output line buffers. The output buffer of the Parallel Input Processor architecture has the same architecture improvement as the Single Input Processor output buffer. The Parallel Input Processor with Two Packet Output Buffers has the highest average throughput per line. The larger output line buffers reduced packet loss at the output line buffers and increased the average throughput per line.

7.3 Total Throughput for Single and Parallel Input Processors Architectures with One Packet and Two Packet Output Buffer Sizes

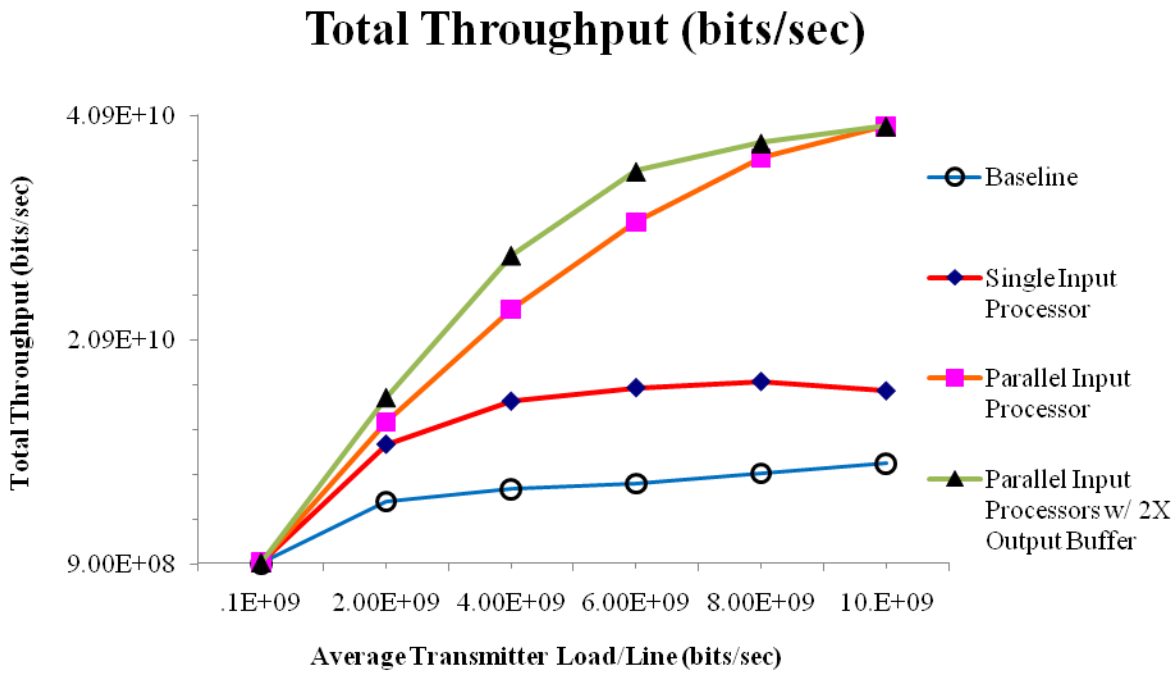

Figure 66 Total Throughput for Baseline, Single Input Processor, Parallel Input Processors Architectures with One Packet and Two Packet Output Buffers Sizes

The total throughput for the Baseline architecture, the Single Input Processor architecture, the Parallel Input Processors architecture, and the Parallel Input Processors architecture with Two Packet Output Buffer is shown above in Figure 66. The Baseline architecture has the lowest total throughput. The total throughput is the lowest for the Baseline architecture because of high packet loss at the forwarding buffer and the output buffer. The Single Input Processor architecture has higher total throughput than the Baseline architecture due to reduced packet loss at the output buffers. The Single Input

Processor architecture has two improvements to its output buffer architecture to reduce packet loss and increase the total throughput. The first improvement is to have one processor per wavelength to forward packets to the next switch or network device. The second improvement is to have one buffer per wavelength resulting in an increase of two additional buffers to delay packets at each output fiber. The Parallel Input Processors architecture has higher total throughput than the Baseline architecture and the Single Input Processor architecture. The higher total throughput is attributed reduced packet loss at the forwarding buffer and the output buffer. Packet loss at the forwarding buffer is reduced by having one forwarding processor per wavelength to forward packets to the output buffer and by having one forwarding buffer per wavelength to delay the incoming packets. The eight processors at the forwarding buffers were able to forward all incoming packets from the eight packet sources into four output lines. The Parallel Input Processors architecture with Two Packet Output Line Buffers has the highest total throughput. The larger output line buffers reduced packet loss at the output line buffers. The reduced packet loss increased the throughput on each output line which increased the total throughput.

Chapter 8 Hypotheses

8.1 Packet Drop for Single Input Processor Architecture

The packet drop for the Single Input Processor architecture is relatively high. The results for packet drop in the Single Input Processor architecture is shown in Table 3 below.

Fiber #		Packet Loss Forwarding Buffer	Packet Loss Output Line Buffer
1	Wavelength 1	2484345	986
1	Wavelength 2		268836
1	Wavelength 3		4736
1	Wavelength 4		32894
2	Wavelength 1	2484000	
2	Wavelength 2		
2	Wavelength 3		
2	Wavelength 4		

Table 3 Packet Drop for Single Input Processor Architecture

Packet drop is high in both forwarding buffers and all output line buffers. Packet drop is improved in the Single Processor architecture with Four Wavelength Conversions as shown in Table 4 below.

Fiber #		Packet Loss Forwarding Buffer	Packet Loss Output Line Buffer
1	Wavelength 1	2483748	0
1	Wavelength 2		0
1	Wavelength 3		0
1	Wavelength 4		0
1	Wavelength 5		0
1	Wavelength 6		0
1	Wavelength 7		0
1	Wavelength 8		0
2	Wavelength 1	2483958	
2	Wavelength 2		
2	Wavelength 3		
2	Wavelength 4		

Table 4 Packet Drop for Single Input Processor Architecture with Four Wavelength Conversion

Packet drop has been eliminated at the output line buffers. Packet drop at the forwarding buffers is still relatively high.

8.2 Statement of Hypotheses

If the forwarding buffer processor can be increased to 40 gigabits per second in the Single Input Processor architecture with Four Wavelength Conversion, packet drop can be eliminated.

8.3 Hypotheses Results

8.3.1 Packet Loss Rate for High Power Single Input Processor vs. Low Power Multiple Input Processors

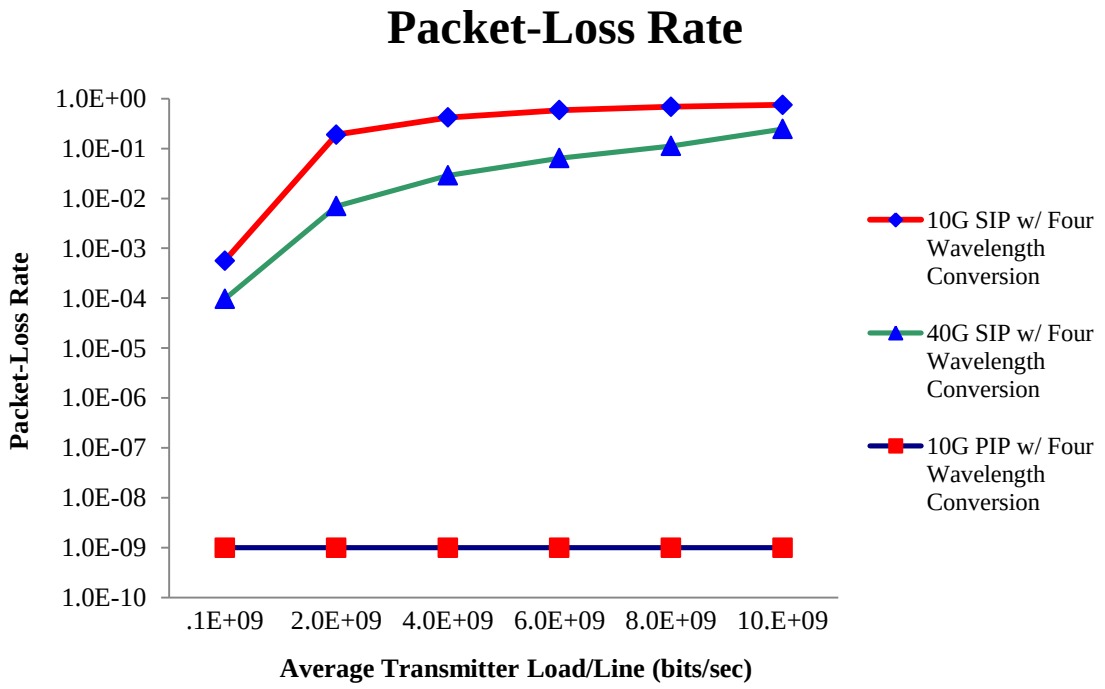

Figure 67 Packet Loss Rate for High Power Single Input Processor vs. Low Power Multiple Input Processors

The packet loss rate for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate, Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 40 gigabit per second packet forwarding rate, and Parallel Input Processors architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second forwarding rate is shown above in Figure 67. The

packet loss rate is the highest for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate due to high packet loss at the forwarding buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the packet forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow the forwarding buffer. The packet loss rate is lower for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 40 gigabit per second packet forwarding rate than the Single Input Processor with Four Wavelength Conversion and a forwarding buffer with a 10 gigabit per second packet forwarding rate. The packet loss rate is high due to high packet loss at the forwarding buffer. In this architecture, the packet forwarding rate for the forwarding buffer processor is equal to the incoming data rate. The forwarding buffer still overflows when three and four packets arrive at the same time or at a higher instanteous data rate than forwarding processor's data rate. The packet loss rate is the lowest for the Parallel Input Processors architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate due to high packet loss at the forwarding buffer. The Parallel Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate does not have any packet loss at the forwarding and output buffers. The Parallel Input Processor architecture has two inprovements to its forwarding buffer archtecture to reduce packet loss. The architecure improvements to the forwarding buffer is to have one forwarding processor per wavelength

and one forwarding buffer per wavelength that can delay two packets. In all three architectures, the packet loss at the output buffers in output Fiber 1 was eliminated by sending the packets coming from input Fiber 2's forwarding buffer to the four wavelength converted lines in output Fiber 1. If the forwarding buffer's processor is increased to 40 gigabits per second in the Single Input Processor architecture with Four Wavelength Conversion, packet drop cannot be eliminated. The buffer size needs to be four times as large as the Parallel Input Processor architecture. The larger buffer size is not available yet. This architecture is not practical. The Parallel Input Processors archtecture with the number of processors equal to the number of incoming lines and the number of wavelength converters equal to the number of incoming wavelengths performs is a better architecture. Hence this is one of the recommended architectures.

8.3.2 Average Throughput per Line for High Power Single Input Processor vs. Low Power Multiple Input Processors

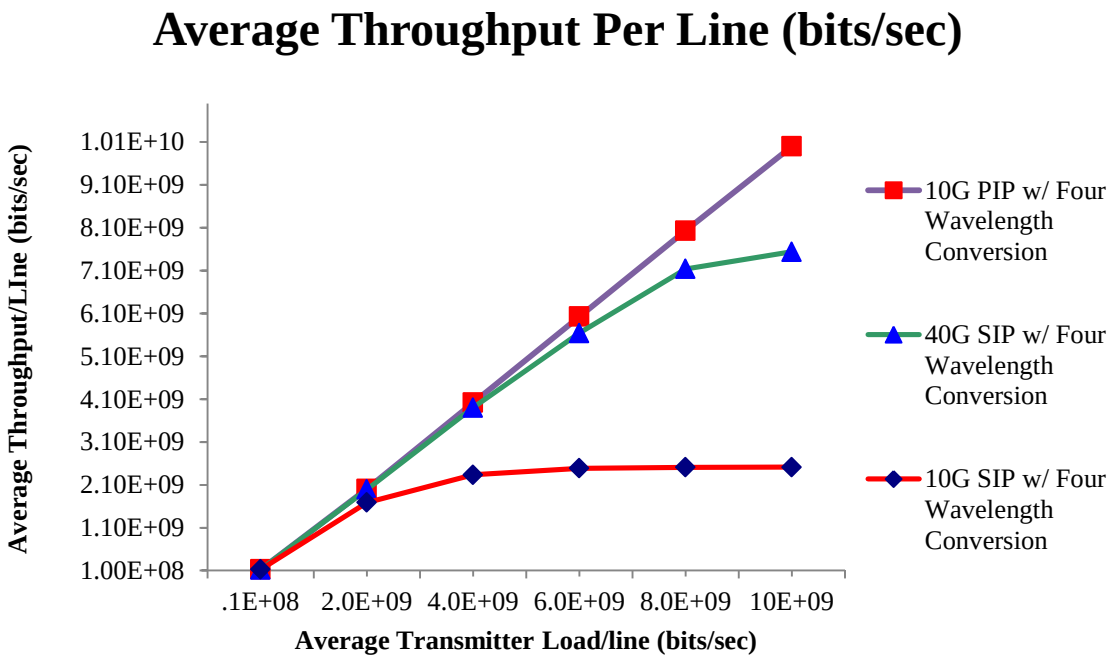

Figure 68 Average Throughput per Line for High Power Single Input Processor vs. Low Power Multiple Input Processors

The average throughput per line for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate, Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 40 gigabit per second packet forwarding rate, and Parallel Input Processors architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second forwarding rate is shown above in Figure 68. The average throughput per line is the lowest for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor

with a 10 gigabit per second packet forwarding rate. The average throughput per line is low because of high packet loss at the forwarding buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the packet forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow the forwarding buffer. The average throughput per line is higher for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 40 gigabit per second packet forwarding rate than the Single Input Processor with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate. The 40 gigabit per second packet forwarding rate for the forwarding buffer processor performed well up to 4 gigabits per second for average tranmitter load per line. Above 4 gigabits per second for the average transmitter load per line, packet loss increased significantly and reduced the average throughput per line from its maximum potential value. The average throughput per line is the highest for the Parallel Input Processors architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate due to high packet loss at the forwarding buffer. The Parallel Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate does not have any packet loss at the forwarding and output buffers. Because of this, there is not any packet loss, the average throughput per line reached its theroretical maximum. The Parallel Input Processor architecture has two inprovements to its forwarding buffer archtecture to reduce packet loss. The architecure improvements to the forwarding

buffer is to have one forwarding processor per wavelength and one forwarding buffer per wavelength that can delay two packets. In all three architectures, the packet loss at the output buffers in output Fiber 1 was eliminated by sending the packets coming from input Fiber 2's forwarding buffer to the four wavelength converted lines in output Fiber 1. The Parallel Input Processors archtecture with the number of processors equal to the number of incoming lines and the number of wavelength converters equal to the number of incoming wavelengths performs very well. Hence this is one of the recommended architectures.

8.3.3 Total Throughput for High Power Single Input Processor vs. Low Power Multiple Input Processors

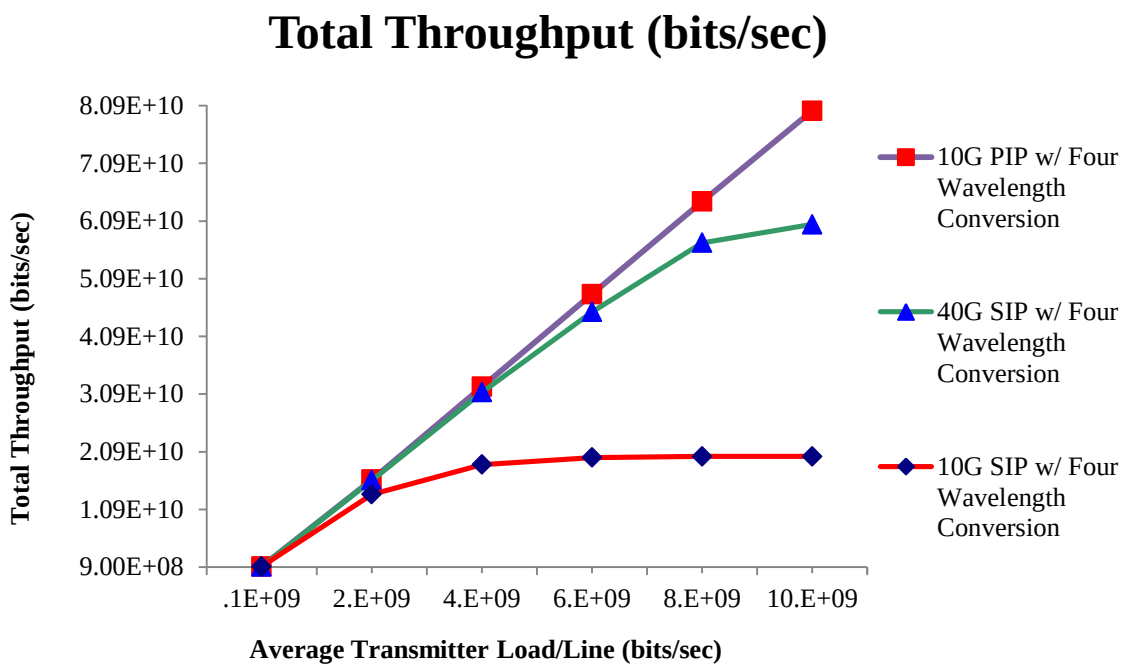

Figure 69 Total Throughput for High Power Single Input Processor vs. Low Power Multiple Input Processors

The total throughput for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate, Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 40 gigabit per second packet forwarding rate, and Parallel Input Processors architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second forwarding rate is shown above in Figure 69. The total throughput is the lowest for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second

packet forwarding rate. The total throughput is low when compared to the Parallel Input Processors with Four Wavelength Conversion and a forwarding buffer processor of 10 gigabits per second because of high packet loss at the forwarding buffer. The packet loss at the forwarding buffer is from incoming packets arriving at a higher rate to the forwarding buffer than the packet forwarding rate of the proccessor for the fowarding buffer causing the packets to overflow the forwarding buffer. The total throughput is higher for the Single Input Processor architecture with Four Wavelength Conversion and a forwarding buffer processor with a 40 gigabit per second packet forwarding rate than the Single Input Processor with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate. The 40 gigabit per second packet forwarding rate for the forwarding buffer processor performed well up to 4 gigabits per second for average tranmitter load per line. Above 4 gigabits per second for the average transmitter load per line, packet loss increased significantly and reduced the total throughput from its maximum potential value. The total throughput is the highest for the Parallel Input Processors architecture with Four Wavelength Conversion and a forwarding buffer processor with a 10 gigabit per second packet forwarding rate. The total throughput is the highest because there is not any packet loss. The total throughput reached its theroretical maximum. The Parallel Input Processor architecture has two inprovements to its forwarding buffer archtecture to reduce packet loss. The architecure improvements to the forwarding buffer is to have one forwarding processor per wavelength and one forwarding buffer per wavelength that can delay two packets. In all three architectures, the packet loss at the output buffers in output Fiber 1 was eliminated by

sending the packets coming from input Fiber 2's forwarding buffer to the four wavelength converted lines in output Fiber 1. The Parallel Input Processors archtecture with the number of processors equal to the number of incoming lines and the number of wavelength converters equal to the number of incoming wavelengths performs very well. Hence this is one of the recommended architectures.

Chapter 9 Recommended Architectures

Given: The input data rate per input line be less than or equal to the processing speed of individual processors

Recommended Architecture # 1

The recommended architecture #1 is Parallel Input Processors/ Parallel Output Processors (one per wavelength) with availability of Next Best Routes (Packet Loss rate almost zero).

Recommended Architecture # 2

The recommended architecture #2 is Parallel Input Processors/ Parallel Output Processors (one per wavelength) with the number of wavelength converters equal to the number of input wavelengths (Packet Loss Rate almost zero).

Chapter 10 Contributions

This dissertation proposes a number of single and parallel processor architectures and protocols for optical packet switching in all optical networks making use of a number of recent advances in high speed processors and optical buffers and a number of packet contention resolution techniques in wavelength, time, and space, alternative routing and processing speeds. The input and output lines can transmit multiple wavelengths per line (i.e., wavelength division multiplexed lines).

All Optical Networks are becoming the dominant infrastructure for high speed communication in ATM, OTN and Internet.. In this dissertation a number of architectures and protocols for optical packet switching in all optical networks are developed, simulated and evaluated. It is shown that some of these architectures can provide excellent performance in terms of packet loss ratio (nearly zero packet loss ratio) and high throughput.

Packet switching will provide a number of advantages over light path establishment method. These advantages are as follows: Firstly, in a large network a light path may consist of interconnection of a number of optical links. Thus establishment, maintenance and simultaneous obligation of all required resources over long light paths may be problematic. This is not required for packet switching. In packet switching packets are transmitted and switched dynamically at each node using the resources available at that node. At any time only the resources needed for connecting to the next node are obligated. Secondly, In case of

congestion a new light path may be needed to be established. Thus in a heavily loaded network frequent establishment and reestablishment of such light paths are needed. On the other hand in packet switching packets can be dynamically routed around congestion by updating routing tables at the nodes. This may lead to lower delay for packets. Thirdly, packet switching uses fewer resources as at any time only the resources between a transmitting node and the next node are in use, whereas in light path method all the resources between all the nodes in a light path are in use as long as the light path is maintained. Fourthly, in light path establishment method sometimes resources may be not be utilized as the whole path need to be maintained irrespective of whether data is transmitted over it or not, whereas in packet switching resources are obligated only when they are used. Thus the results of this dissertation will provide these benefits by enabling implementation of optical packet switching in all optical networks.

Optical packet switching techniques developed in this dissertation will enable high performing large optical transport network (OTN) structure to be constructed. The OTN can comprise of the interconnection of a number of optical cross connects (OXC) in mesh architectures.. Each interconnecting optical fiber will support multiple wavelengths. There will also be many optical fibers. The number of optical fibers may be on the order of 10 – 30 optical fibers per switch. Thus very high total capacity on the network can be realized. The optical cross connects (OXC) using optical packet switches will support many thousands of optical channels. The optical packet switch network will be able to provide channels to

clients such as IP routers, synchronous optical network / synchronous digital hierarchy (SONET/SDH) network elements, and asynchronous transfer mode (ATM) switches and OTN.

The optical packet switch will maximize utilization of network resources. This reduces the number of resources required for the optical network. The optical packet switch will be used as an edge router interfacing to the optical transport network (OTN) and the internet protocol (IP) network.

Chapter 11 Conclusions

A number of architectures and protocols for high-speed optical packet switching have been developed, simulated, and performance evaluated in terms of packet loss ratio, average throughput per line, and total throughput. The architectures and protocols are developed by using high-speed processors for contention reduction and a number of contention resolution schemes in time, wavelength, space, higher processing power, and multiple WDM channels per fiber.

Thirteen architectures were simulated and evaluated for 10 Gbps input lines and processor speed of 10 Gbps. Out of these architectures only two architectures have excellent performance (nearly zero packet loss and high throughput).

One of the architectures has Parallel (one per input line) Input and Output Processors with available Next Best Route. The second architecture has Parallel Input and Output Processors with the number of spare channels available at the output for wavelength conversion be equal to the number of input channels.

In these two cases, the packet loss ratio is almost zero at the input line rate of 10 Gbps for optical buffer size of 793 ns and lookup rate of 213.4 Mlps

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